

PAMS Technical Documentation

NHX-7 Transceiver

Chapter 2

Baseband Module JP3

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System Module JP3: Introduction

This document specifies the System module JP3 of the NHX-7 ETACS cellular phone.

The JP3 System Module comprises the baseband and the RF functions of the phone.

Baseband Sub-module

The Baseband submodule controls the internal operation of the phone. It controls the user interface, i.e. LCD driver, keyboard and audio interface functions. The module performs all signalling towards the system and carries out audio-frequency signal processing. In addition, it controls the operation of the transceiver and stores tuning data for the phone.

The baseband architecture is basically similar to the previous generation. However, the system specified logical voltage level used is 2.82V and new features include a improved charging circuit CHAPS and a new power supply circuit PSA.

The baseband architecture supports a power saving function called "extended standby mode". This sleep mode shuts off the Receiver and part of the NASTA blocks. The phone is woken up at every FOCC:s first word and it is "sleeping" the rest of the time.

The nominal battery voltage in NHX-7 is 3.6V. The actual battery voltage varies between 3.0 to 4.2V/5.3V depending on the used cell type (Li-Ion or NiMH) and whether the phone is connected to a charger (limit on 5.3V with NiMH battery in idle).

Battery charging is controlled by a PWM signal from the MCU. The PWM duty cycle is determined by a charging software. The PWM signal is fed to the CHAPS charging switch and through the charging pins to an external charger. There can be two types of chargers connected to the phone.

Standard chargers (two wires) provide coarse supply power, which is switched by the CHAPS for suitable charging voltage and current. Advanced chargers (three wires) are equipped with a control input, through which the phone gives PWM charging control signal to the charger.

Block Diagram of baseband

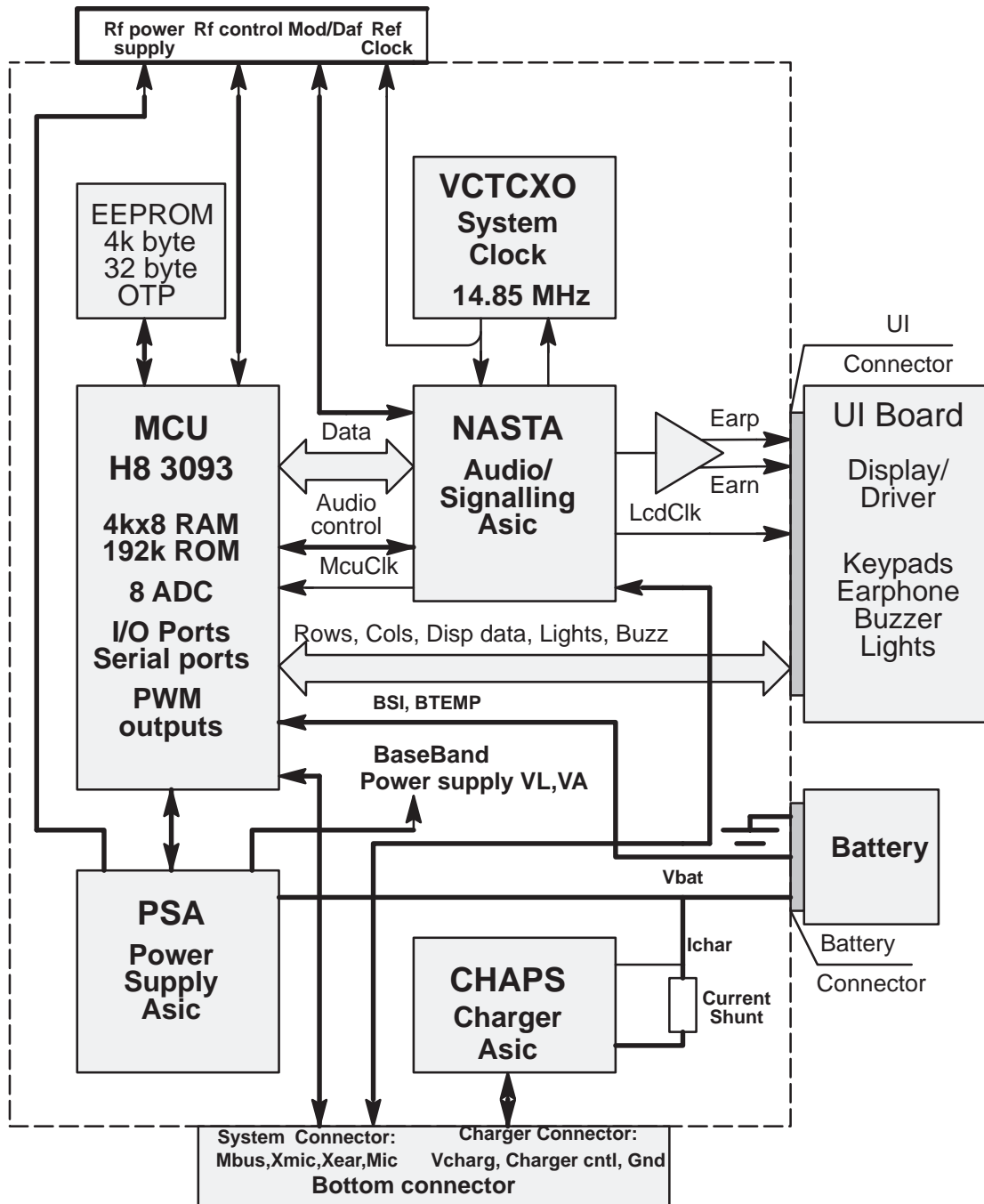


Figure 1.

Technical summary

The baseband module consists of VCTCXO module and four ASIC circuits, PSA, CHAPS, NASTA 4.5, EEPROM, and some standard circuits, DUAL BILATERAL SWITCH (TC7W66F), AUDIO POWER AMPLIFIER (LM4862) and a Hitachi H8 series controller (H8/3093 MCU).

The MCU includes memories, 192 kbytes ROM and 4 kbytes RAM. It controls all transceiver functions.

The EEPROM type is 4 kbytes with 32 bytes. The OTP memory is a serial I²C-bus type.

The baseband is running from a 2.8 V power rail, which is supplied by a power controlling asic. In the PSA asic there are two separate power supplies for BaseBand (VA,VL) and two externally controllable power supplies for RF (VRX, VTX).

The CHAPS is a charging control ASIC. It is essentially an integrated power switch for controlling charging current, in a mobile phone. CHAPS is designed for 3 cell Nickel or 1 cell Lithium battery packs.

The NASTA circuit integrates the Audio and Modem operations. Because the NASTA supports only one microphone, there are two bilateral switches to connect the internal microphone or the headset microphone to the NASTA MIC input. There is an audio power amplifier for EAR and XEAR lines each. The internal earphone amplifier is a dual ended type output which is in EAR line and there is transistor buffer in XEAR line.

The VCTCXO module is a voltage and temperature controlled oscillator which operates as system clock for RF and BaseBand.

All functional blocks of the baseband are mounted on a single multi layer printed circuit board. All components of the baseband are surface mountable. This board contains also the RF-parts. The B-cover side (battery side) EMC shielding is implemented by using a metallic RF-shields on the RF-blocks. On the other side the engine is shielded with a aluminium frame, which makes a contact to a ground ring of the engine board and a ground plane of the UI-board.

The connections from BaseBand to UI board are fed through a 28-way 2-row board to board spring connector.

Modes of Operation

Power off, Standby, Listening and Conversation modes.

- In Power off mode only the circuits needed for power up are supplied.
- In Standby mode the MCU and needed blocks of the NASTA are active.
- In Listening mode the receiver and some blocks of the NASTA are active.
- In Conversation mode all ICs are active.

CTRLU Circuit

The Control block CTRLU controls all functions of the phone.

Block Description

– CTRLU – PWRU

CTRLU controls the watchdog timer in PSA. It sends a negative pulse at approximately 0,1 s to XPWROFF pin of the PSA to keep the power on. If CTRLU fails to deliver this pulse, the PSA will remove power from the system. When power off is requested CTRLU leaves PSA watchdog without reset. After the watchdog has elapsed PSA cuts off the supply voltages from the phone. CTRLU controls also the charger on/off switching in the PWRU block. Battery charging is controlled by CSW line, which is PWM-controlled output port.

– CTRLU – AUDIO

Interface between microcontroller and the NASTA circuit is bidirectional 8-bit data bus with 4 address lines. Address, data and control lines are used in microcontroller as I/O-port pins. Data lines direction must be controlled with microcontroller data direction register. Interface includes address outputs NA0–3, data inputs (read) / outputs (write) ND0–7, chip select control output XNCS, read control output XNRD, write control output XNWR and interrupt input XINT. To minimize power consumption, control signals XRD and XCS should be in '0' state and address output NA0–3 and NWR in '1' state and data lines ND0–7 should be inputs. Buzzer is controlled by BUZZ_DRV PWM signal. Headset adapter is detected by HSCONN input.

– CTRLU – UIF and DISPLAY

Keyboard is connected directly to the controller. COL 0:3 are output lines and ROW 0:3 are input lines. Watchdog is updated same time with keyboard scanning (XPWROFF). Keyboard scanning is done by driving one COL to 0 V at time and ROWs are used to read which key is pressed.

Keyboards lights are controlled by KEYBLIGHT signal and LCD lights by LCDBLIGHT signal.

LCD controller interface to microcontroller is a bidirectional data line LCDDA, data serial clock line SCLK output, chip select control LCDENX output, command or display data control LCDDC output and reset control LCDRES output.

– CTRLU – RECEIVER

Received signal strength is measured over the RSSI line and intermediate frequency is measured over the IF line.

RX synthesizer and receiver are powered on/off by PSBS_EN line.

– CTRLU – SYNTHESIZER

Frequency is controlled by the AFC signal. The synthesizer is controlled via the synchronous serial bus SDAT/SCLK. The data is latched to the synthesizer by the positive edge of the SLE line. The TX synthesizers power on/off is controlled by VTX_ENA signal.

– CTRLU – TRANSMITTER

The transmitter on/off state is detected over the TXI line. The TXE line activates the power module. The power is controlled via the TXC line which is a PWM-controlled output port (frequency about 9.4 kHz).

Extended standby mode for power saving

The extended standby mode is automatically activated when the phone is working in the control channel (FOCC). The NASTA runs this function, switching on/off the receiver's power supply.

PSPS_EN signal:

– The signal connects the RX regulator on via the PSA when it is in "1" state, in "0" state the RX regulator is off.

HPD_EN signal:

– The signal controls the RX synthesizers hardware power down function.

When it is in "1" state the RX synthesizer is powered up, in "0" state the RX synthesizer is powered down.

Main Components

MCU

The H8/3093 is a CMOS microcontroller. All the memory needed (192kB ROM, 4kB RAM) except the EEPROM, is located in the controller. The MCU operating clock (2.4 MHz) is generated on the NASTA and the VCTCXO. The H8/3093 is operating in single-chip normal mode (mode 3) 192kbyte address space, so all input/output pins are used as I/O-ports.

| Pin Number | Port | Signal | Description |
|------------|------|---------------|-------------------------------|
| 1 | PB0 | SDAT | Synthesizer data line |
| 2 | PB1 | RSSI_READY | RSSI readings synchronization |
| 3 | PB2 | VIBRA_CONTROL | Vibra alerting device on/off |
| 4 | PB3 | RXD | M2BUS net free timer input |
| 5 | PB4 | EAREN | Earphone amplifier enable |
| 6 | PB5 | XPWROFF | Power off control |
| 7 | PB6 | PWRON | Power button state |
| 8 | PB7 | SLE | Synthesizer latch enable |
| 9 | P90 | TXD | Serial interface (M2BUS) |

| Pin Number | Port | Signal | Description |
|------------|--------------------------|-------------|------------------------------------|
| 10 | P92 | RXD | Serial interface (M2BUS) |
| 11 | P94 | ECLK | Serial data clock for EEPROM |
| 12 | VSS | GND | |
| 13 – 20 | P30 – P37 | ND0 – ND7 | Parallel data bus for NASTA |
| 21 | VCC | VL | |
| 22 | P10 | NA0 | Address line for NASTA |
| 23 | P11 | NA1 | Address line for NASTA |
| 24 | P12 | NA2 | Address line for NASTA |
| 25 | P13 | NA3 | Address line for NASTA |
| 26 | P14 | XNCS | NASTA chip select |
| 27 | P15 | XNWR | Write control to NASTA |
| 28 | P16 | XNRD | Read control to NASTA |
| 29 | P17 | LIGHTS | Keypad backlight control |
| 30 | VSS | GND | |
| 31 – 34 | P20 – P23 | COL0–COL3 | Keypad outputs |
| 35 – 38 | P24 – P27 | ROW0 – ROW3 | Keypad inputs (Input pullup used) |
| 39 | P50 | SCLK | Serial data clock for lcd driver |
| 40 | P51 | LCDENX | Chip select signal for lcd driver |
| 41 | P52 | LCDDC | Display or Command data |
| 42 | P53 | LCDSDA | Data line for lcd driver |
| 43 | P60 | VTX_ENA | TX synthesizer enable. Active high |
| 44 – 45 | MD0 – MD1 | | Mode selection |
| 46 | NC | NC | |
| 47 | $\overline{\text{STBY}}$ | VL | |
| 48 | RES | XRES | Reset from PSA |
| 49 | NMI | NC | |
| 50 | VSS | GND | |
| 51 | EXTAL | CLKMCU | External system clock from NASTA |
| 52 | XTAL | NC | |
| 53 | VCC | VL | |
| 54 | P63 | TXE | Transmitter on/off |
| 55 | P64 | LIM | Battery cut off limit selection |

| Pin Number | Port | Signal | Description |
|------------|------|-----------|------------------------------------|
| 56 | P65 | XEAR_EN | Headset earpiece amplifier control |
| 57 | RESO | NC | |
| 58 | AVSS | GND | |
| 59 | P70 | VBATSW | Battery voltage |
| 60 | P71 | VCHARG | Charger voltage |
| 61 | P72 | ICHAR | Charging current measurement |
| 62 | P73 | BTEMP | Battery temperature |
| 63 | P74 | RSSI | Received signal strength |
| 64 | P75 | TXI | Transmitter state monitor |
| 65 | P76 | HSCON | Headset detecting voltage |
| 66 | P77 | BSI | Battery size indicator |
| 67 | VREF | VA | |
| 68 | AVCC | VA | |
| 69 | P80 | XINT | Interrupt request from NASTA |
| 70 | P81 | LCDRES | LCD reset signal |
| 71 | P82 | LCDBLIGHT | LCD backlight control |
| 72 | P83 | HEADSW | Headset switch indicator |
| 73 | PA0 | MIC_EN | Internal microphone control |
| 74 | PA1 | LCDCLK | LCD clock from NASTA |
| 75 | PA2 | BUZZ_DRV | PWM output for buzzer |
| 76 | PA3 | SCLK | Serial clock for synthesizer |
| 77 | PA4 | CSW | Charging control PWM |
| 78 | PA5 | EDATA | Eeprom data line |
| 79 | PA6 | TXC | Transmitter power control |
| 80 | PA7 | XMIC_EN | Headset microphone control |

EEPROM

There is one 4kbyte EEPROM with 32byte OTP memory in the phone. The EEPROM is a nonvolatile memory in which the tuning data for the phone is stored. In addition, it contains the short code memory locations to retain user selectable phone numbers. The OTP memory is ROM area for identification and security purposes.

Table 1. EEPROM signals:

| Pin No | Signal | Description |
|--------|--------|----------------------------|
| 5 | SDA | I ² C bus data |
| 6 | SCL | I ² C bus clock |

PWRU Circuit

Power Distribution

The main components of the Power Unit are the PSA (Power Supply Asic) and the CHAPS (Charger Power Switch).

In normal operation the baseband is powered from the phone's battery. The battery consists of three Nickel Metal Hydride cells. There is also a possibility to use batteries consisting of one Lithium-Ion cell. An external charger is used for recharging the battery and supplying power to the phone. The charger can be either a standard charger that can deliver around 400 mA or a so called performance charger, which can deliver supply current up to 850 mA.

The baseband contains components that control the power distribution to the whole phone excluding those parts that use continuous battery supply. The battery feeds power directly to three parts of the system: PSA, RF-power amplifier, and UI (buzzer and display and keyboard lights).

The power management circuit CHAPS provides protection against over-voltages, charger failures and pirate chargers etc. that could otherwise cause damage to the phone.

Table 2. DC Characteristics of PWRU signals

| Signal name | From To | Parameter | Minimum | Typical | Maximum | Unit | Function |
|-------------|--------------------|----------------|---------|---------|---------|------|--------------------------------|
| VBATT | Battery RF/UIF | Voltage | 3.0 | 3.6 | 5.0/5.3 | V | Supply voltage for RF and UIF |
| | | Current | | | 3500 | mA | |
| XRES | PSA MCU,NAS-TA,UIF | Logic high "1" | 0.7*VL | | VL | V | PSA is Power On Mode |
| | | Logic low "0" | 0 | | 0.3*VL | V | PSA is Power Off or Reset Mode |

Table 2. DC Characteristics of PWRU signals (continued)

| Signal name | From To | Parameter | Minimum | Typical | Maximum | Unit | Function |
|---|----------------------|----------------------------|--------------|---------|---------|------|---|
| LIM | MCU CHAPS | Logic high "1" | VL-0.5 | | VL | V | Cutoff limit 5.0 V |
| | | Logic low "0" | 0 | | 0.4 | V | Cutoff limit 4.6 V |
| XPWRON | UIF PSA | Logic high "1" | 0.7* VBAT | | VBAT | V | Power On switch open |
| | | Logic low "0" | 0 | | 1.2 | V | Power On switch closed |
| XPWR OFF | MCU PSA | Logic high "1" | VL-0.5 | | VL | V | Watchdog counter not reset |
| | | Logic low "0" | 0 | | 0.4 | V | Watchdog counter reset "1" -> "0" |
| PWRON | PSA MCU | Logic high "1" | 0.7*VL | | VL | V | PSA is in Power On Mode |
| | | Logic low "0" | 0 | | 0.3*VL | V | PSA is in Power Off or Reset mode |
| PSBS_EN (Phone Supported Battery Save) | NASTA PSA | Logic high "1" | 2.0 | | 2.90 | V | VRX Enabled |
| | | Logic low "0" | 0 | | 0.5 | V | VRX Disabled |
| HPD_EN | NASTA PLL circuit | Logic high "1" | 2.0 | | 2.90 | V | Hardware power down disabled on PLL circuit |
| | | Logic low "0" | 0 | | 0.4 | V | Hardware power down enabled on PLL circuit |
| VTX_ENA | MCU PSA | Logic high "1" | VL-0.5 | | VL | V | TX VCO and synthesizer powered on |
| | | Logic low "0" | 0 | | 0.4 | V | TX VCO and synthesizer powered off |
| VBATSW | PSA MCU | Voltage | 0 | | 2.45 | V | Switched internally divided VBAT voltage |
| | | VBATSW/VBAT division ratio | 0.436 | 0.45 | 0.464 | | |
| VCHARG | PSA MCU | Voltage | 0 | | 2.8 | V | Switched Charger voltage |
| | | VCHRSW switch resistance | 0 | 0.25 | 1.0 | Kohm | |
| ICHAR | AMPLIFIER MCU | Voltage | 0 | | 2.90 | V | Charger Current Measurement over the shunt resistor. |
| TXD | MCU PSA | Logic high "1" | VL-0.5 | | VL | V | M2BUS data output, PSA M2BUS output is in high-Z state. |
| | | Logic low "0" | 0 | | 0.4 | V | M2BUS data output, PSA M2BUS output is LOW |

Table 2. DC Characteristics of PWRU signals (continued)

| Signal name | From To | Parameter | Minimum | Typical | Maximum | Unit | Function |
|-------------|------------|----------------|---------|---------|---------|------|---|
| RXD | PSA MCU | Logic high "1" | 2.0 | | 2.90 | V | M2BUS data input |
| | | Logic low "0" | 0 | | 0.5 | V | |
| CSW | MCU PSA | Logic high "1" | 2.0 | | 2.90 | V | Charger switch and ACP-9 control signal |
| | | Logic low "0" | 0 | | 0.5 | V | |
| | | PWM frequency | 1 | | 32 | Hz | |
| | | PWM duty cycle | 0 | | 100 | % | |

Battery charging

Acceptable chargers are detected by the software. The absolute maximum input voltage is 30V due to the transient suppressor that is protecting the charger input. At the phone end there is no difference between a plug-in charger or a desktop charger. The DC-jack pins and bottom connector charging pads are connected together inside the phone. The charging block diagram is below.

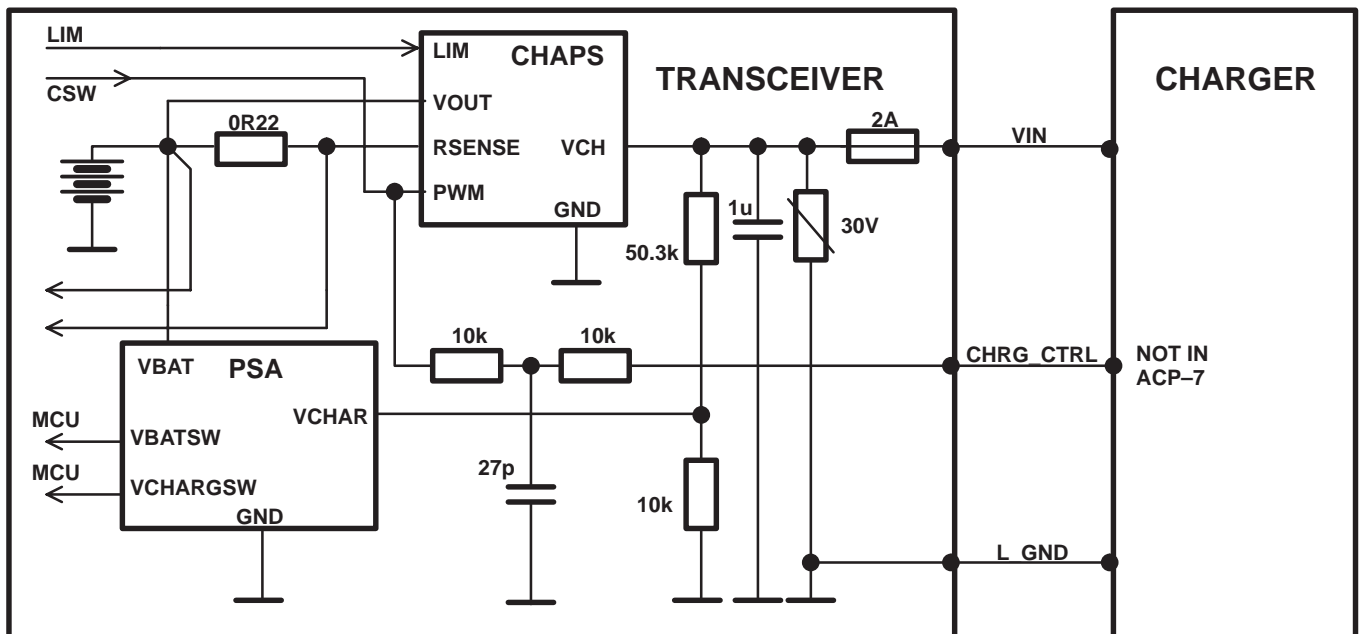


Figure 2. Charging block diagram

Startup charging

When a charger is connected, the CHAPS is supplying a startup current minimum of 130mA to the phone. The startup current provides initial

charging to a phone with an empty battery. The startup circuit charges the battery until the battery voltage level reaches 3.0V (+/- 0.1V) and the PSA releases the PURX reset signal and program execution starts. Charging mode is changed from startup charging to PWM charging that is controlled by the MCU software. If the battery voltage reaches 3.55V (3.75V maximum) before the program has taken control over the charging, the startup current is switched off. The startup current is switched on again when the battery voltage has decreased to 100mV (nominal).

Table 3. Startup characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------|------|------|------|------|
| VOUT Start– up mode cutoff limit | Vstart | 3.45 | 3.55 | 3.75 | V |
| VOUT Start– up mode hysteresis NOTE: Cout = 4.7 uF | Vstarthys | 80 | 100 | 200 | mV |
| Start–up regulator output current VOUT = 0V ... Vstart | Istart | 130 | 165 | 200 | mA |

Battery overvoltage protection

Output overvoltage protection is used to protect phone from damage. This function is also used to define the protection cutoff voltage for different battery types (Li or Ni). The power switch is immediately turned OFF if the voltage in VOUT rises above the selected limit VLIM1 or VLIM2.

Table 4. VLIM characteristics

| Parameter | Symbol | LIM input | Min | Typ | Max | Unit |
|---|--------|-----------|-----|-----|-----|------|
| Output voltage cutoff limit (during transmission or Li–battery) | VLIM1 | LOW | 4.4 | 4.6 | 4.8 | V |
| Output voltage cutoff limit (no transmission or Ni–battery) | VLIM2 | HIGH | 4.8 | 5.0 | 5.2 | V |

The voltage limit (VLIM1 or VLIM2) is selected by logic LOW or logic HIGH on the CHAPS (N101) LIM– input pin. Default value is lower limit VLIM1.

When the switch in output overvoltage situation has once turned OFF, it stays OFF until the the battery voltage falls below VLIM1 (or VLIM2) and PWM = LOW is detected. The switch can be turned on again by setting PWM = HIGH.

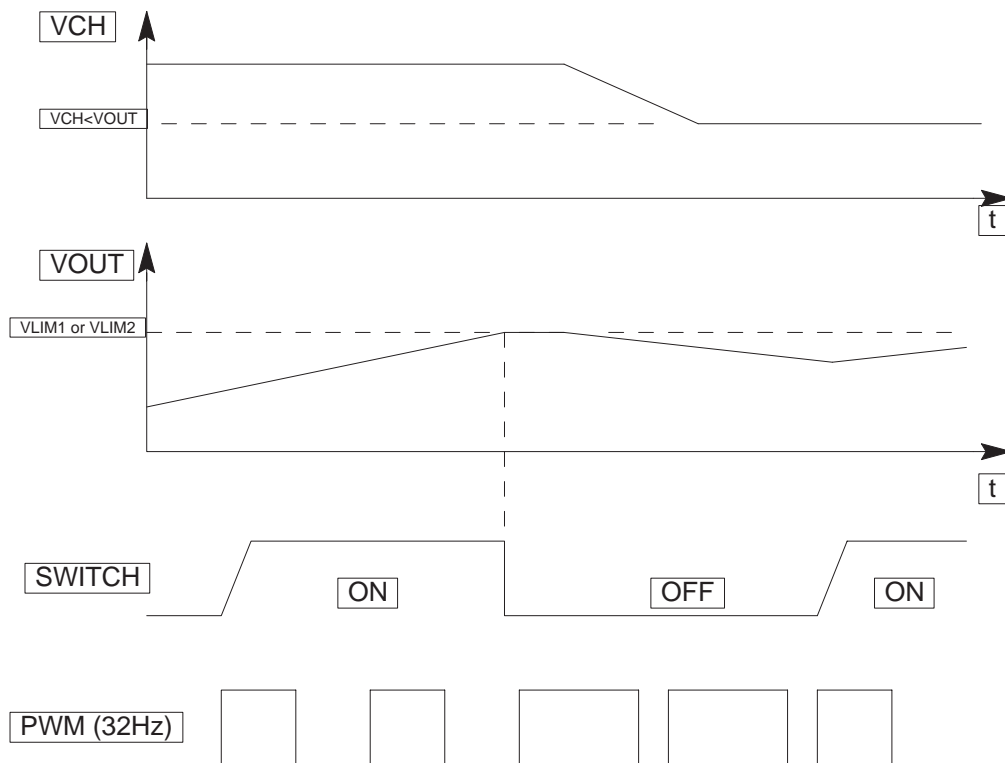
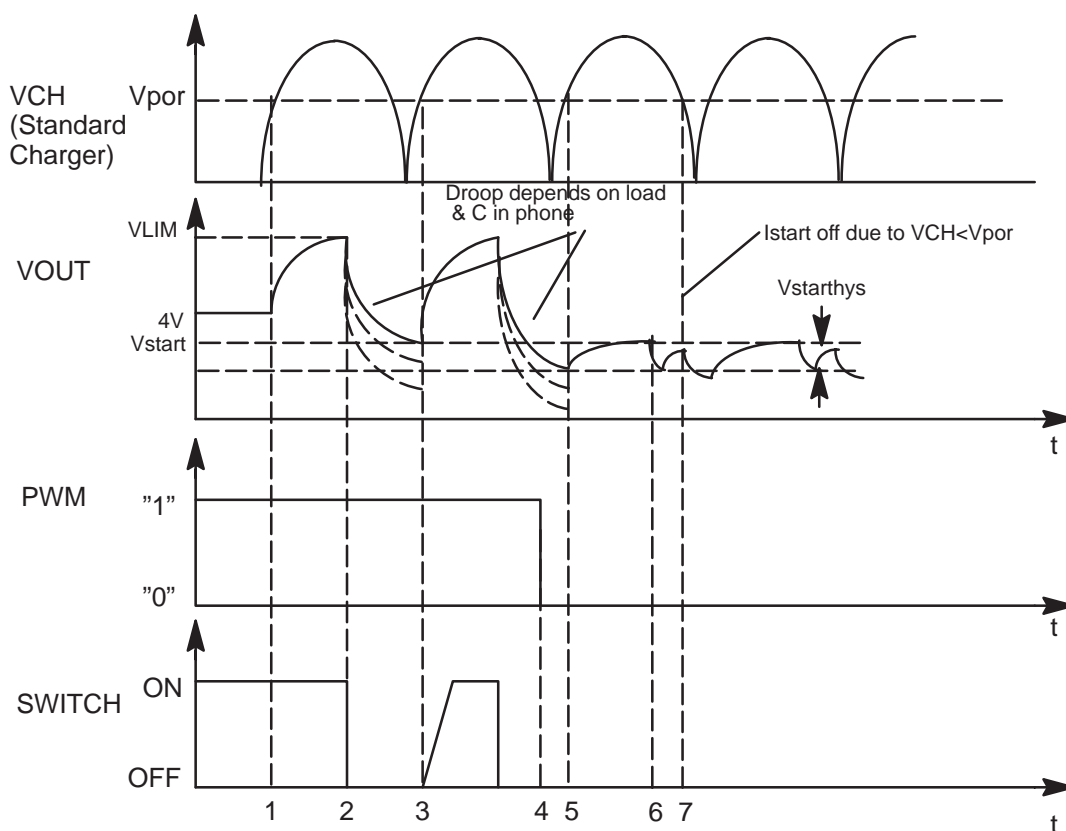


Figure above: Battery overvoltage protection

Battery removal during charging

Output overvoltage protection is also needed in case the main battery is removed when a charger connected or a charger is connected before the battery is connected to the phone.

With a charger connected, if V_{OUT} exceeds V_{LIM1} (or V_{LIM2}), the CHAPS turns switch OFF until the charger input has decreased below V_{por} (nominal 3.0V, maximum 3.4V). The MCU software stops the charging (turn off PWM) when it detects that the battery has been removed. The CHAPS remains in protection state as long as the PWM stays HIGH after the output overvoltage situation has occurred.



1. Battery removed, (standard) charger connected, VOUT rises (follows charger voltage)
2. VOUT exceeds limit VLIM(X), switch is turned immediately OFF
3. VOUT falls (because no battery), also $V_{CH} < V_{por}$ (standard chargers full-rectified output). When $V_{CH} > V_{por}$ and $V_{OUT} < VLIM(X)$ -> switch turned on again (also PWM is still HIGH) and VOUT again exceeds VLIM(X).
4. Software sets PWM = LOW -> CHAPS does not enter PWM mode
5. PWM low -> Startup mode, startup current flows until Vstart limit reached
6. VOUT exceeds limit Vstart, Istart is turned off
7. VCH falls below Vpor

Figure above: Battery removal during charging

Different PWM frequencies (2Hz and 32 Hz)

When a travel charger (2-wire charger) is used, the power switch is turned ON and OFF by the PWM input when the PWM rate is 2Hz. When the PWM is HIGH, the switch is ON and the output current $I_{out} = I_{charger} - I_{CHAPS}$. When PWM is LOW, the switch is OFF and the output current $I_{out} = 0$. To prevent the switching transients inducing noise in audio circuitry of the phone soft switching is used.

The performance travel charger (3-wire charger) is controlled with PWM at a frequency of 32Hz. When the PWM rate is 32Hz CHAPS keeps the power switch continuously in the ON state.

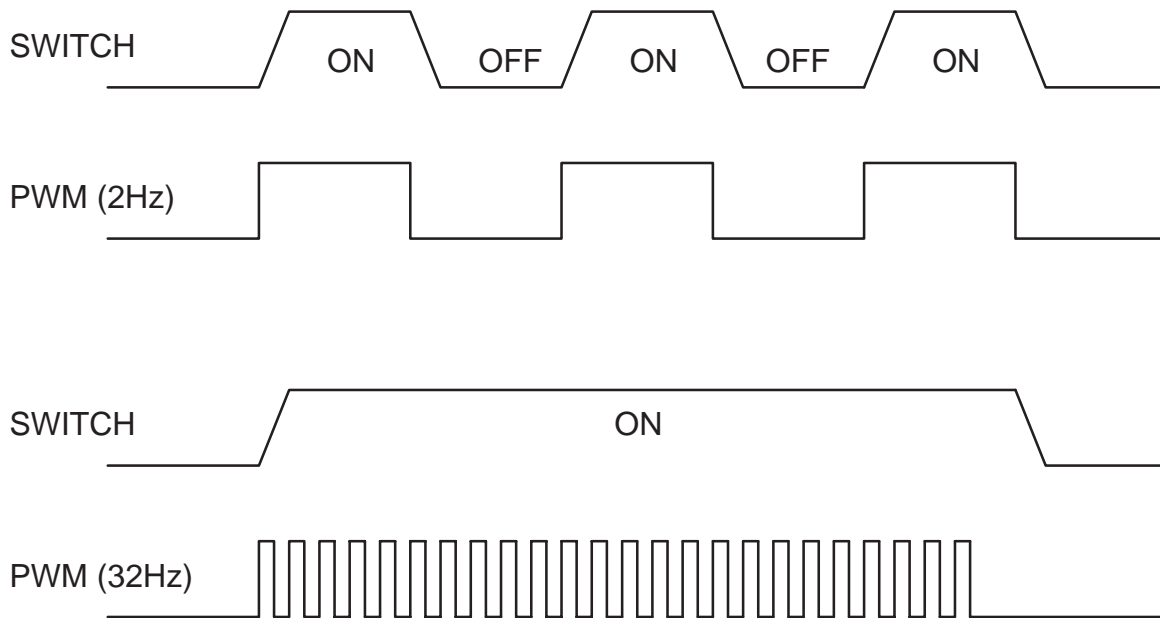


Figure 3. Switch control with 2Hz and 32 Hz frequencies (in this case 50% duty cycle)

Charger Current measurement

The charging current measurement is based on the reading of differential voltages over the shunt resistor at the CHAPS output lines. The voltage is measured and amplified by a differential amplifier and it is carried to the MCU A/D converter. Measurement area is up to 1400 mA and 1 A/D bit equals 1.85 mA. The charging current calibration is done with 0 mA and 500 mA in production test line. When charger is connected the current measurement connection is activated. The A/D-conversion result and charging current can be calculated from equations :

$$A/D \text{ readout} = 1024 * V_{IC\text{HAR}} / V_{REF}$$

Charging current:

$$I = (V_{IC\text{HAR}} - V_{IC\text{HAR}}(0\text{mA})) * (500\text{mA} / (V_{IC\text{HAR}}(500\text{mA}) - V_{IC\text{HAR}}(0\text{mA})))$$

where $V_{REF} = 2.82 \text{ V}$
 $V_{IC\text{HAR}}$ = voltage in ICHAR line

Table 5. Charger current measurement

| Name | Min | Typ | Max | Unit | Notes |
|--------------------|------|------|------|------|---|
| V _{ICHAR} | 0.46 | 0.69 | 0.92 | V | Charging current is 0 mA. (Calibration point) |
| | 163 | 250 | 334 | A/D | |
| | 1.22 | 1.44 | 1.65 | V | Charging current is 500 mA. (Calibration point) |
| | 443 | 522 | 598 | A/D | |
| | 1.98 | 2.19 | 2.39 | V | Charging current is 1000 mA. |
| | 718 | 795 | 867 | A/D | |

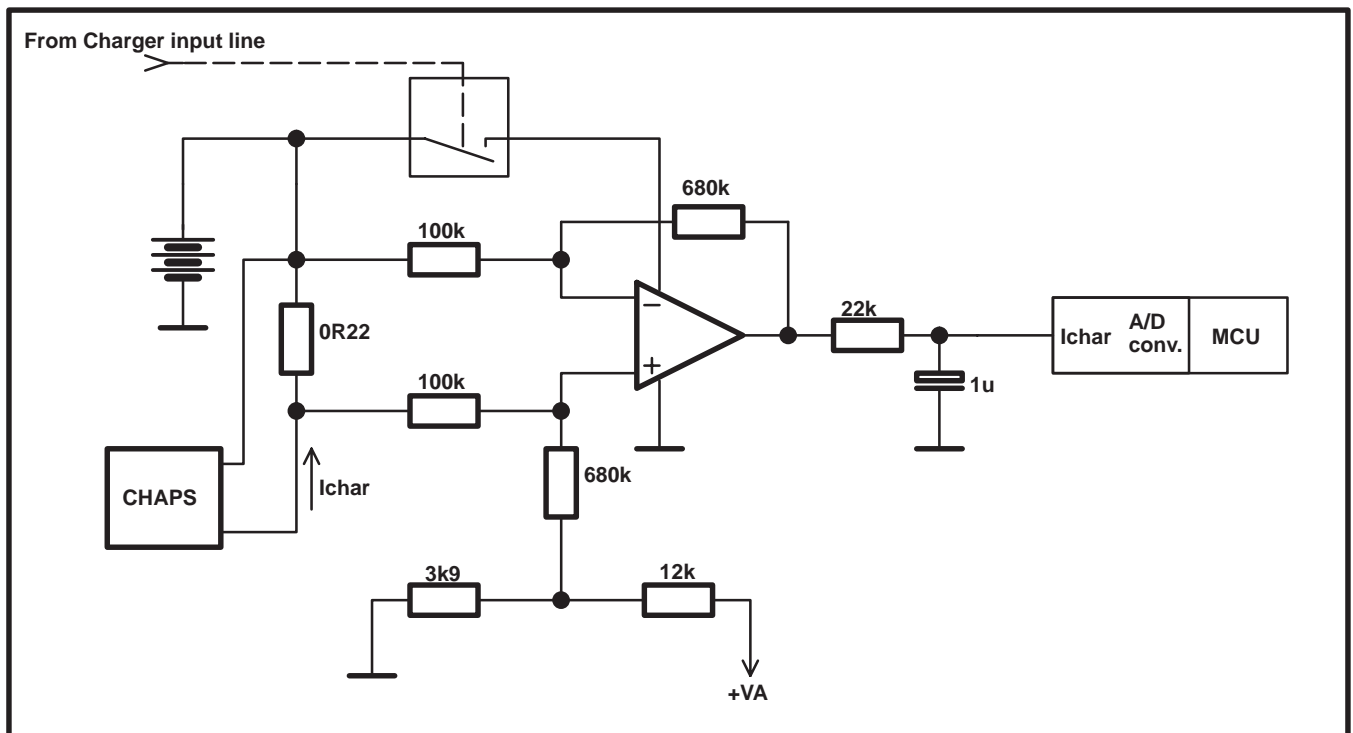


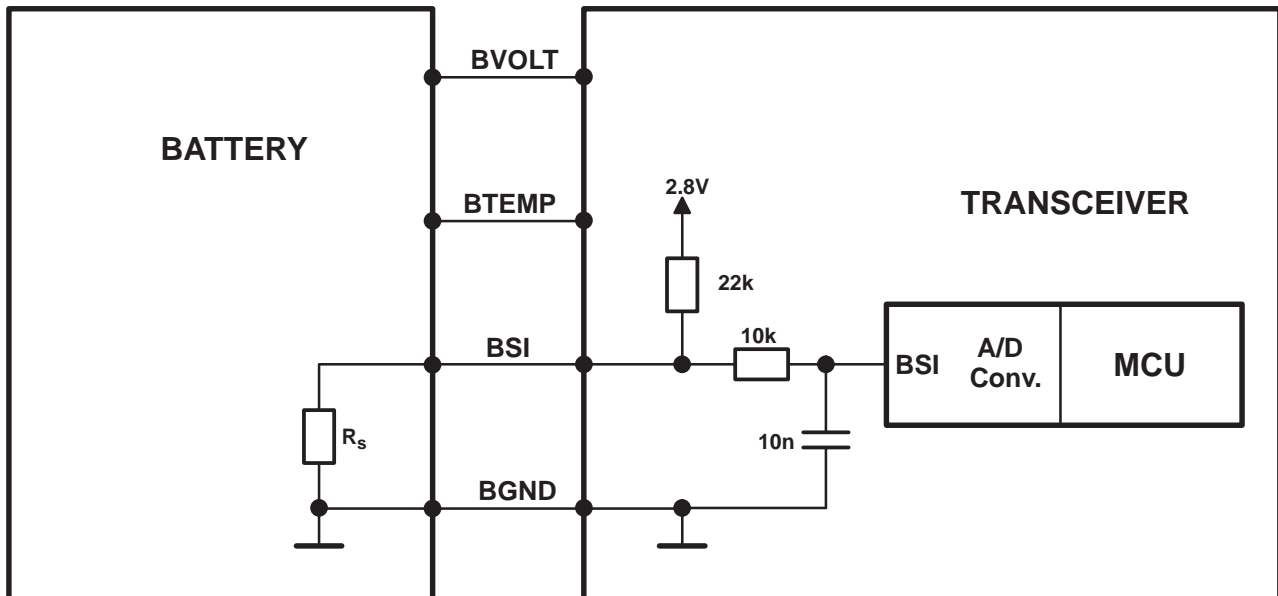
Figure 4. Charger current measurement

Battery identification

Different battery types are identified by a pull-down resistor inside the battery pack. The BSI line inside transceiver has a 22k pull-up to VA. The MCU can identify a battery by reading the BSI line DC-voltage level with a MCU (D201) A/D-converter.

Table 6. Battery Identification

| Name | Min | Typ | Max | Unit | Notes |
|------|------|-----|------|------|---|
| BSI | 0 | | 2.8 | V | Battery size indication 22k pullup resistor to VA in phone |
| | 14.2 | 15 | 15.8 | kohm | Indication of a BMS-2V vibra battery (900mAh NiMH) |
| | 9.5 | 10 | 10.5 | kohm | Indication of a BMS-2S battery (900mAh NiMH) |
| | 37 | 39 | 41 | kohm | Indication of a BLS-2 battery (900mAh Lilon) |
| | 48.5 | 51 | 53.5 | kohm | Indication of a BLS-4 battery (1600mAh Lilon) |
| | -5 | | 5 | % | Indication resistor and pullup resistor tolerance |



Battery voltage measurement, VBATSW

Battery voltage can be measured up to 6.27 V from the VBATSW line. The absolute accuracy is low because of the voltage reference and A/D-converter +/- 8 LSB accuracy . This battery voltage measurement offset error must be calibrated with input voltage 4.1 V. The A/D conversion result can be calculated from equation:

$$A/D \text{ readout} = 1024 * (VBAT * (0.45)) / VREF \quad VREF=2.82 \text{ V}$$

For example:

| | | |
|-------|---------|------------|
| 4.1 V | results | 670 = 29Dh |
| 3.6 V | results | 588 = 24Ch |
| 3.0 V | results | 490 = 1EAh |

Charger voltage measurement, VCHARG

Charger voltage can be measured up to 17.00 V from VCHARG line. The absolute accuracy is low because of the voltage reference and A/D-con-

verter ± 8 LSB accuracy. The A/D-conversion result can be calculated from equation :

$$\text{A/D readout} = 1024 * (\text{VCHARG} * (10/60.3)) / \text{VREF} \quad \text{VREF} = 2.82 \text{ V}$$

For example:

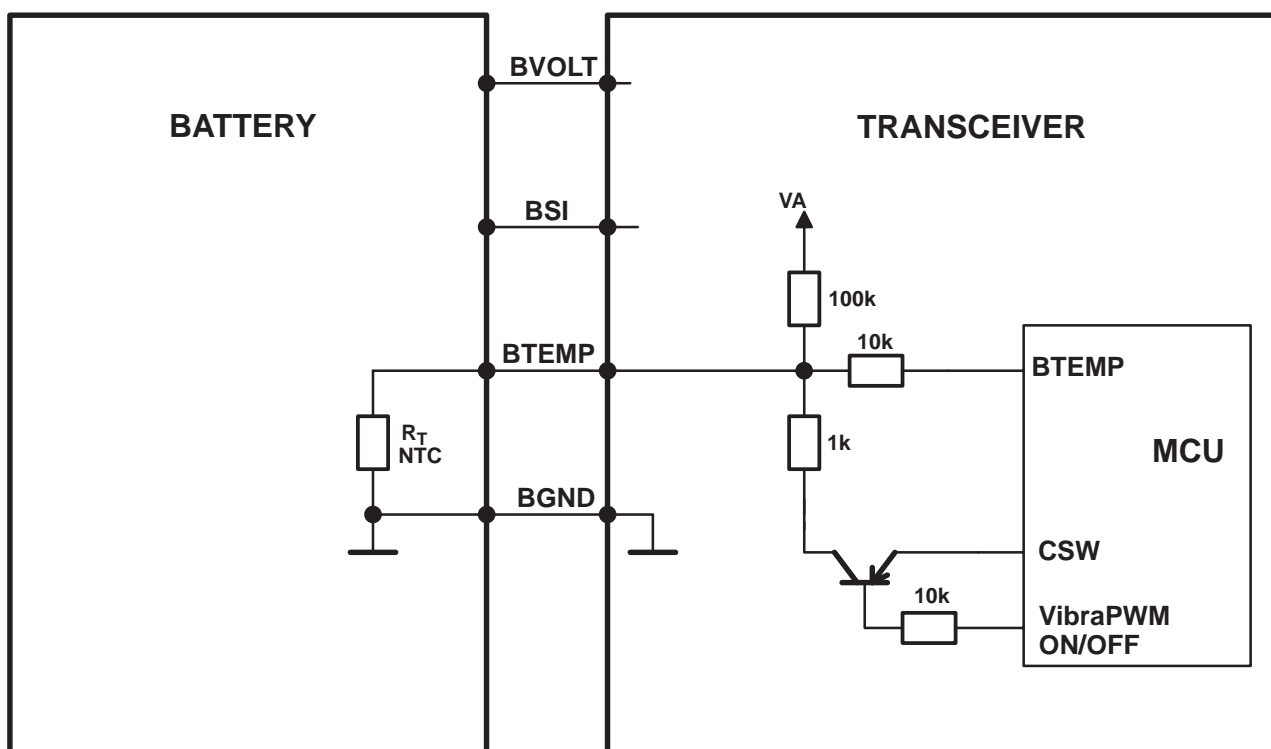
$$8.4 \text{ V} \quad \text{results} \quad 506 = 1\text{F9h}$$

Battery temperature

The battery temperature is measured with a NTC inside the battery pack. The BTEMP line inside transceiver has a 100k pullup to VA. The MCU can calculate the battery temperature by reading the BTEMP line DC-voltage level with a MCU (D201) A/D-converter.

Table 7. Battery temperature

| Pin | Name | Min | Typ | Max | Unit | Notes |
|-----|-------|-----|-----|------|------|---|
| 3 | BTEMP | 0 | | 2.90 | V | Battery temperature indication 100k pullup resistor to VA in phone Battery package has NTC pull down resistor: 47k $\pm 5\%$ @ +25C , B=4050 $\pm 3\%$ |
| | | -1 | | 1 | % | 100k pullup resistor tolerance |



Battery temperature monitoring schematic diagram above

Based on $47\text{k}\Omega \pm 5\%$ NTC with $B = 4090 \pm 1.5\%$. Without any alignment, with that and 1% pull-up resistor, $\pm 2.5\text{ }^\circ\text{C}$ accuracy is achieved between -20 and $+60\text{ }^\circ\text{C}$ ($\pm 3.5\text{ }^\circ\text{C}$ @ $-40 \dots +85\text{ }^\circ\text{C}$).

Table 8. Battery temperature vs. AD readings and NTC resistance

| T [°C] | AD | R [kΩ] | T [°C] | AD | R [kΩ] | T [°C] | AD | R [kΩ] |
|--------|-----|--------|--------|-----|--------|--------|-----|--------|
| -40 | 963 | 1589 | 5 | 560 | 120.9 | 50 | 145 | 16.53 |
| -35 | 942 | 1151 | 10 | 497 | 94.53 | 55 | 122 | 13.63 |
| -30 | 915 | 842.8 | 15 | 436 | 74.40 | 60 | 103 | 11.30 |
| -25 | 882 | 622.6 | 20 | 379 | 58.95 | 65 | 88 | 9.404 |
| -20 | 842 | 464.1 | 25 | 327 | 47.00 | 70 | 74 | 7.865 |
| -15 | 795 | 349.0 | 30 | 280 | 37.71 | 75 | 63 | 6.607 |
| -10 | 743 | 264.6 | 35 | 238 | 30.43 | 80 | 54 | 5.573 |
| -5 | 685 | 202.3 | 40 | 202 | 24.70 | 85 | 46 | 4.721 |
| 0 | 623 | 155.8 | 45 | 171 | 20.15 | 90 | 39 | 4.015 |

Vibra alerting device

A vibra alerting device is used for giving silent signal to the user of an incoming call. The device is not placed in the phone but it will be added to a special battery pack. The vibra is controlled with a PWM signal by the MCU via the BTEMP battery terminal.

Table 9. Vibra battery connection

| Name | Min | Typ | Max | Unit | Notes |
|-------|------|-----|------|------|--|
| BTEMP | 9 | 11 | 14 | kHz | PWM control to VIBRA BATTERY |
| BSI | 0 | | 2.90 | V | Battery size indication Phone has 100kohm pull up resistor. |
| | 14.2 | 15 | 15.8 | kohm | Battery size indication resistor (vibra battery) |

A 15kohm BSI resistor is needed to detect the vibra battery. It is only used to enable vibra selection in user menu. When alerting, VibraPWM signal is delivered to battery.

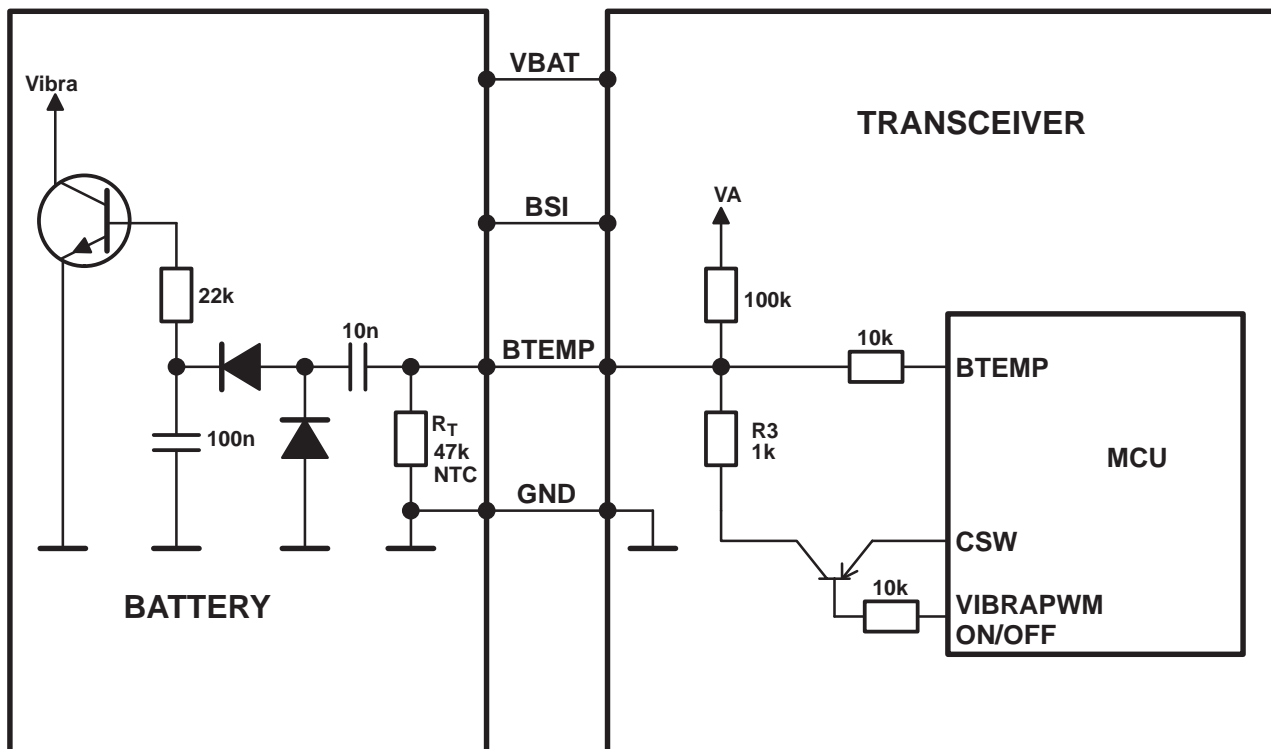


Figure 5. Vibra battery

Supply voltage regulators and controlling

The heart of the power distribution is the PSA asic. It includes all the voltage regulators and feeds power to the whole system. The baseband digital and analog parts are powered from the VL and VA regulators which provide the 2.82 V baseband supply. The baseband regulators are active when the phone is powered on.

The PSA includes also two 2.82 V regulators (VRX and VTX) providing power to the RF section. These regulators can be controlled by the direct control signals from the MCU. The VRX regulator can also be controlled by the signal from the NASTA.

- VTX_ENA (from MCU) controls VTX regulator
- PSBS_ENA (from NASTA) controls VRX regulator

In addition PSA includes also functions listed bellow:

- Buffer for the M2BUS.
The buffer translates the logical input signal to open-drain output.

Table 10. M2BUS buffer truth table

| Input | Output |
|-------|--------|
| LOW | LOW |
| HIGH | Z |

- Power on/off and reset logic. The Power off logic can be used as a watchdog.
- Supply voltage monitor and automatic reset/power-off.
VBATSW is internally divided and buffered battery voltage output. The A/D –converter input monitoring the battery voltage can be connected here. The circuit monitors the voltage at the VBAT input and forces the circuit to Reset if the voltage level is below allowed limit voltage, VBATcoff–. A hysteresis is included to prevent oscillation between different states.
- Battery charger detection.
Externally divided charger voltage VCHAR goes through PSA internal switch to VCHARSW output. The A/D –converter input monitoring the charger voltage can be connected here.
- Automatic on–chip current limiting
- On–chip thermal shutdown, which protects PSA from overheating.
Thermal shutdown includes hysteresis in order to prevent oscillation during the thermal protection.

Table 11. Regulators VA and VL characteristic

| Parameter Test Conditions | Symbol | Limits | | | Unit |
|--|----------------------------|--------|--------------------------|--------------------------|--|
| | | Min | Typ | Max | |
| Output Voltage | VL, VA | 2.73 | 2.82 | 2.90 | V |
| Output current of the regulator (all regulators enabled) | I_{outVL} I_{outVA} | 0 | | 40 100 | mA mA |
| Quiescent current VL: $I_{load} = 0mA$ $I_{load} = 40mA$ VA: $I_{load} = 0mA$ $I_{load} = 100mA$ | I_q | | | 200 220 200 220 | μA μA μA μA |
| Quiescent current $T_{amb} = +25^{\circ}C$, VBAT=3.6V VL: $I_{load} = 0mA$ $I_{load} = 40mA$ VA: $I_{load} = 0mA$ $I_{load} = 100mA$ | I_q | | 110 130 110 130 | | μA μA μA μA |
| Quiescent current in Power–Off VL VA | I_{qoff} | | | 6 15 | μA μA |
| Line regulation: VL, VA $I_{outVL} = 40mA$, $I_{outVL} = 100mA$, $3.25V \leq VBAT \leq 5.2V$ | V_{Lline} , V_{Aline} | | | 20 | mV |
| Load regulation: VL, VA $0mA \leq I_{loadVL} \leq 40mA$, $0mA \leq I_{loadVA} \leq 100mA$, $3.25V \leq VBAT \leq 5.2V$ | V_{Lload} , V_{Aload} | | | 30 | mV |

Table 11. Regulators VA and VL characteristic (continued)

| Parameter Test Conditions | Symbol | Limits | | | Unit |
|---|-------------------------------------|-----------|-----|------------|---------------|
| | | Min | Typ | Max | |
| Line transient: AC=0.5V square wave Slew rate = 50 mV/ μ s f = 500Hz ... 2kHz $3.5V \leq V_{BAT} \leq 5.2V$ | $V_{L_{linetr}}$, $V_{A_{linetr}}$ | 40 | | | dB |
| Load transient: VL, VA $I_{load_{VL}}$ 100 μ A to 40mA, $I_{load_{VA}}$ 100 μ A to 100mA in 10 μ s $3.25V \leq V_{BAT} \leq 5.2V$ | ΔV Trec Note 1 | | | 40 20 | mV μ s |
| Current limit (VL, VA = 0V) VL VA | I_{lim} | 60 150 | | 180 450 | mA mA |
| Power Supply Ripple Rejection $3.2V \leq V_{BAT} \leq 5.2V$ $0mA \leq I_{load_{VL}} \leq 40mA$, $0mA \leq I_{load_{VA}} \leq 100mA$ f = 10Hz ... 10kHz | PSRR | 40 | | | dB |
| Settling time Cload=1 μ F \pm 20% load current 0mA | t_s Note 2 | | | 160 | μ s |

Note 1: Voltage deviation (ΔV) is the output voltage overshoot in transient response. Recovery time (Trec) is the time from the beginning of the transient response to the time point when the regulator output voltage first crosses the final stable value after overshoot.

Note 2: Settling time is defined from the time point of mode change Power-Off to Reset to the time when regulator output voltage is within 5% of the final value.

Table 12. Regulators VRX and VTX characteristic

| Parameter Test Conditions | Symbol | Limits | | | Unit |
|---|------------------------------------|--------------|------|--------------------------|--|
| | | Min | Typ | Max | |
| Output Voltage | VRX, VTX | 2.73 | 2.82 | 2.90 | V |
| Output currents of the regulators (all regulators enabled) | $I_{out_{VRX}}$ $I_{out_{VTX}}$ | 0.05 0.02 | | 50 60 | mA mA |
| Quiescent current VRX: $I_{load} = 0A$ $I_{load} = 50mA$ VTX: $I_{load} = 0A$ $I_{load} = 60mA$ | I_q | | | 320 360 320 360 | μ A μ A μ A μ A |

Table 12. Regulators VRX and VTX characteristic (continued)

| Parameter Test Conditions | Symbol | Limits | | | Unit |
|---|---|----------|--------------------------|----------------|----------------------|
| | | Min | Typ | Max | |
| Quiescent current Tamb = +25°C, VBAT=3.6V VRX: Iload = 0A Iload = 50mA VTX: Iload = 0A Iload = 60mA | Iq | | 180 195 180 195 | | μA μA μA μA |
| Quiescent current in Power-Off VRX VTX | Iqoff | | | 14 17 | μA μA |
| Line regulation: VRX, VTX IoutVRX = 50mA, IoutVTX = 60mA, 3.25V ≤ VBAT ≤ 5.2V | VRX _{line} , VTX _{line} | | | 20 | mV |
| Load regulation: VRX, VTX 50μA ≤ Iload _{VRX} ≤ 50mA, 20μA ≤ Iload _{VTX} ≤ 60mA, 3.25V ≤ VBAT ≤ 5.2V | VRX _{load} , VTX _{load} | | | 30 | mV |
| Line transient: VRX, VTX AC=0.5Vpp square wave Slew rate = 50 mV/μs f = 500Hz 2kHz 3.5V ≤ VBAT ≤ 5.2V | VRX _{inetr} , VTX _{inetr} | 40 | | | dB |
| Load transient: VRX, VTX Iload _{VRX} 50μA to 50mA, Iload _{VTX} 20μA to 60mA in 10μs 3.25V ≤ VBAT ≤ 5.2V | ΔV Trec Note 1 | | | 40 20 | mV μs |
| Current limit (VRX, VTX = 0V) VRX VTX | I _{lim} | 75 90 | | 225 270 | mA mA |
| Power supply ripple rejection 3.25V ≤ VBAT ≤ 5.2V 50μA ≤ Iload _{VRX} ≤ 50mA, 20μA ≤ Iload _{VTX} ≤ 60mA, f = 10Hz.....10kHz f = 10Hz.....50kHz f = 10Hz.....100kHz | PSRR _{VRX, VTX} | | | 50 40 35 | dB dB dB |
| Settling time, Cload=1μF±20% load current 0mA | ts Note 2 | | | 100 | μs |

Note 1: Voltage deviation (ΔV) is the output voltage overshoot in transient response. Recovery time (Trec) is the time from the beginning of the transient response to the time point when the regulator output voltage first crosses the final stable value after overshoot.

Note 2: Settling time is defined from VTX_ENA/VRX_ENA rise to the time when regulator output voltage is within 5% of the final value.

Operation modes

The circuit has three operational modes: Power-Off, Reset and Power-On. The additional modes are the Protection mode and Battery disconnected ($V_{BAT} < V_{Rth}$, master reset threshold). Respective conditions of the external signals are described in the NO TAG.

Table 13. Operational modes

| MODE | PURX | VRX_EN A | VTX_EN A | VL VA | VRX | VTX | VBATSW | VCHAR -SW | PWRON- BUFF |
|-----------|------|-------------|-------------|----------|------|------|--------|--------------|----------------|
| Power-Off | LOW | X | X | Z | Z | Z | Z | Z | LOW |
| Reset | LOW | L | L | 2.8V | Z | Z | Z | Z | LOW |
| | LOW | H | H | 2.8V | 2.8V | 2.8V | Z | Z | LOW |
| Power-On | HIGH | L | L | 2.8V | Z | Z | VBATSW | VCHAR | XPWRONX |
| | | H | H | 2.8V | 2.8V | 2.8V | VBATSW | VCHAR | XPWRONX |

NOTE: VBATSW and VCHARSW are controlled by internal VSW_ENA-signal during power-on.

NOTE: PWRONBUFF is an inverted (and buffered) PWRONX. A logic LOW level at PWRONX (active LOW) will force a logic HIGH level at PWRONBUFF.

Power-Off Mode

In order to be in Power-Off mode V_{BAT} must be above V_{Rth} .

During Power-Off mode PURX is at logical low level. VA, VL, VRX and VTX regulators are disabled and in high-Z low output state.

Entering Power-Off Mode

The PSA contains a watchdog counter that is reset by writing "1" – "0" sequence to input PWROFFX.

The circuit goes to Power-off mode from Power-On after delay T_{off} if watchdog has not been reset during this time.

The other possibility to enter the Power-Off is from Reset, if the PSA can not enter Power-On mode because $V_{BAT_{coff+}}$ is not reached. This means that watchdog elapses before the microcontroller is able to produce a pulse to PWROFFX. If charger is present ($V_{CHAR} > V_{CHAR_{th}}$), transition from Reset to Power-Off can not occur but the circuit stays in Reset mode as long as battery has been charged above $V_{BAT_{coff+}}$.

The circuit goes to battery disconnected mode if battery voltage drops below master reset threshold (V_{Rth-}).

For testing purposes the watchdog can be disabled and reset by grounding the WD_DISX pin. In normal use it can be left floating (internal pull up).

Charging in Power–Off

Charging is not possible in Power–Off. Connecting a charger during Power–Off generates a rising edge on VCHAR input and the circuit enters Reset mode. Circuit stays in Reset as long as the battery is charged to the limit $V_{BATcoff+}$.

If the watchdog elapses during Power–On when charger is connected, the circuit goes to Power–Off. Because charger detection is level sensitive, charger is detected and the circuit goes via Reset mode to Power–On mode.

Reset Mode

The circuit goes into Reset mode from Power–Off when:

- the battery voltage is initiated (master reset) or
- logic low voltage in PWRONX is detected or
- charger voltage becomes available or
- when recovering from Protection mode

In Reset mode the VL and VA outputs are activated by an internal enable signal. The VRX and VTX have external enable inputs VRX_ENA and VTX_ENA. VBATSW and VCHARSW are disabled and PURX is LOW.

The circuit leaves the Reset mode after a delay T_{rd} for Power–On if $V_{BAT} > V_{BATcoff+}$. Watchdog is reset when Power–On mode is entered.

The circuit goes into Reset mode from Power–On when the battery voltage VBAT drops below $V_{BATcoff-}$.

VBAT is monitored internally, hence if voltage VBAT drops below the threshold (determined by internal resistors), transition from Power–on to Reset mode is done. If VBAT doesn't rise back above reset release limit in time T_{off} the Watchdog elapses and the circuit powers off.

To avoid PSA going to RESET mode due to fast transient, transition from Power–On to Reset mode is not done if VBAT is below $V_{BATcoff-}$ for shorter time than threshold detection delay T_{dd} .

The circuit leaves the Reset mode after a delay T_{rd} if $V_{BAT} > V_{BATcoff+}$.

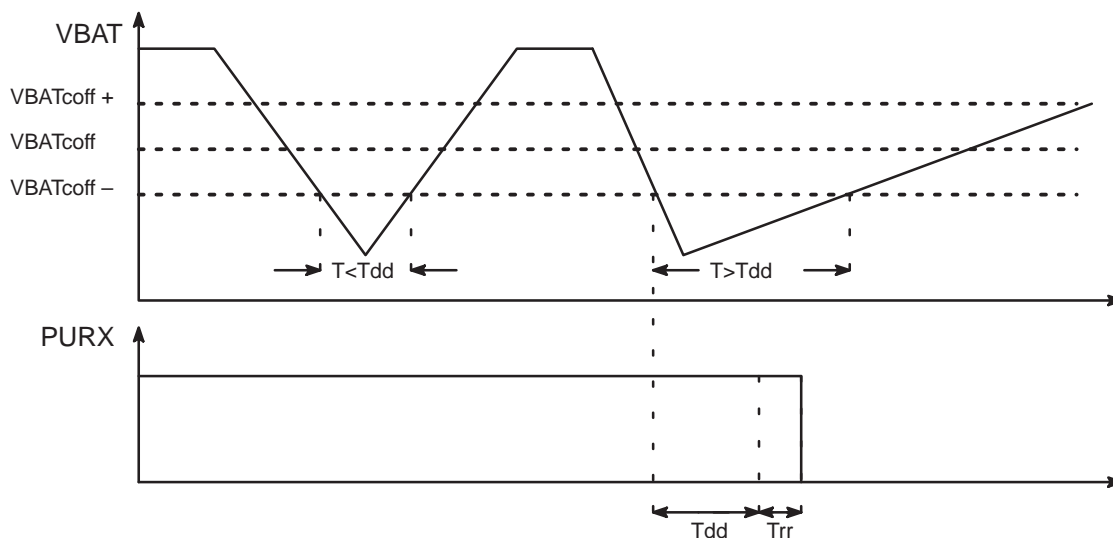


Figure 6. Threshold detection delay T_{dd} and PURX reaction time T_{rr}

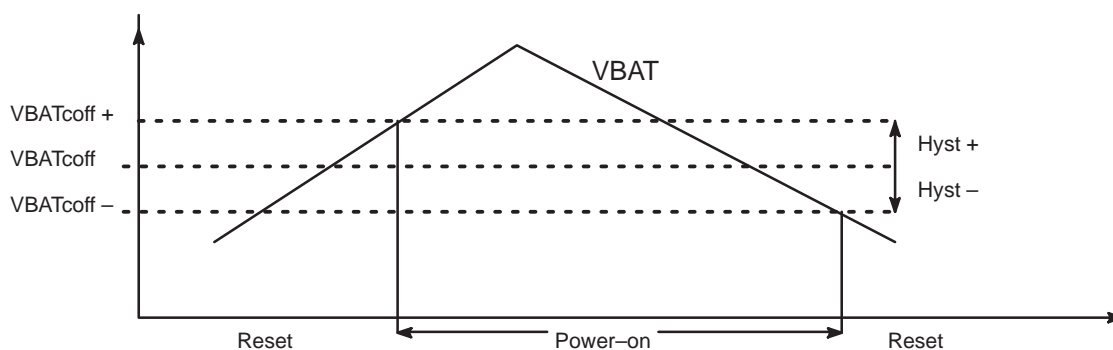


Figure 7. Reset limits and hysteresis

Power-On Mode

In Power-on mode all the functions are active. VBATSW and VCHARSW outputs are activated by the internal enable signal VSW_ENA. PURX is high in Power-On.

From Power-On mode the circuit goes to Power-Off mode after a delay T_{off} (watchdog delay set by an external capacitor C_{osc}) if no writing sequence to PWROFFX from logical high level to low level has detected during this time.

In Power_on mode the circuit does not react on PWRONX pulse i.e. the circuit must be switched off by the system by not updating the watchdog writing in time T_{off} .

AUDIO

Audio Control

Most of audio control is performed by the NASTA 4.5 IC, which contains audio and signalling processors. Internal and headset microphones signals are connected to same input of the NASTA via bilateral switch. The EAR signal of the NASTA is fed to an external amplifier (LM4862) with a dual ended type output. The XEAR signal of NASTA is carried to the transistor buffer.

Internal microphone

The internal microphone is connected to the bottom connector by means of mounting springs for automatic assembly. The microphone requires a bias current to operate. The bias current is generated in the NASTA.

Internal earphone

The internal earphone is connected to the UI board. The low impedance, dynamic type earphone is connected to a differential output of the audio amplifier (LM4862). Keypress and user function response beeps are generated with the internal earphone.

Buzzer

Alerting tones and/or melodies as a signal of an incoming call are generated with a buzzer that is controlled with a PWM signal by the MCU. The buzzer is a SMT device and is placed on the UI board.

Headset detection

The external headset device is connected to the system connector, from which the signals are routed via bilateral switch to the NASTA microphone input and via transistor buffer to the NASTA XEAR output. In the XMIC line there is a 47 k Ω pullup in the transceiver. Resistance of the microphone is low compared to the transceiver pullup. When there is no call going the XMIC is pulled up. When a headset is connected, the XMIC is pulled down. The XMIC is connected to HSCON line which is one of MCU's A/D inputs. MCU is scanning the HSCON line and it detects both connection and disconnection. When headset is detected the headset microphone will get the DC bias current from transistor V740.

Headset Switch detection

In the XEAR line there is a 47 k Ω pullup in the transceiver. Resistance of the earphone is low compared to the transceiver pullup. When a remote

control switch of the headset is open, there is a capacitor in series with the earphone, so the XEAR is pulled up by the phone. When the switch is closed, the XEAR is pulled down via the earphone. The XEAR is connected to HEADSW which is one of MCU input line. So both press and release of button gives an interrupt.

NASTA ASIC

The NASTA 4.5 is a single chip audio/signalling processor in a 64 TQFP package for AMPS and TACS systems.

Main features

- Single chip 2.8 V supply and Internal signal ground generation
- 8 bit parallel interface with pull ups
- Low noise microphone amplifier
- Input for a handset microphone or an accessory
- Microphone sensitivity compensation +4.8/–4.2 dB range (4 bits)
- Compressor
- RX and TX filters
- Tx hard limiters
- Internal reference compensation +1.00/–0.75 dB range(3 bits)
- Summing stage for voice and signalling data and SAT and ST
- Transmitter compensation amplifier with +3.75/–3.75 dB range (4 bits)
- TX speech max deviation trimmer with +1.75/–1.75 dB range (3 bits)
- Receiver compensation amplifier with +3.75/–3.75 dB range (4 bits)
- Volume control amplifier with –20/+17.5 range (4 bits)
- Earphone amplifier with drive capability for ceramic earpiece
- Buffered output for a handset or an accessory
- Audio mute switches
- Dual and single tone multifrequency generator
- 4.8 MHz oscillator/PLL–VCO circuitry for clock generation
- Driver for buzzer amplifier
- Hardware implemented hands free
- Synchronization to the received wide band signalling from base station
- Data validity detection
- Continuous word sync validity check
- Manchester encoding and decoding
- 3/5 majority vote and bch decoding for the received messages
- SAT filtering, detection and regeneration
- ST signal generation
- Transmitted data,ST and SAT filtering
- Programmable output clock with clock stop
- Low power consumption modes, Extended standby drivers
- Programmable timer
- AFC function

Table 14. Pin list of the NASTA ASIC

| Pin no | Symbol | Pin type | Notes |
|--------|-------------|----------|--|
| 1 | VDD1 | | + 2.8 V Supply voltage, digital |
| 2 | XRD | DIN/pu | Read control signal, active state LOW, pull-up > 50 k Ω |
| 3 | XCS | DIN/pu | Chip select signal, active state LOW, pull-up > 50 k Ω |
| 4 | A3 | DIN | 4-bit address bus, MSB |
| 5 | A2 | DIN | 4-bit address bus |
| 6 | A1 | DIN | 4-bit address bus |
| 7 | A0 | DIN | 4-bit address bus, LSB |
| 8 | D7 | DIO | 8-bit bidirectional data bus MSB |
| 9 | D6 | DIO | 8-bit bidirectional data bus |
| 10 | D5 | DIO | 8-bit bidirectional data bus |
| 11 | D4 | DIO | 8-bit bidirectional data bus |
| 12 | D3 | DIO | 8-bit bidirectional data bus |
| 13 | D2 | DIO | 8-bit bidirectional data bus |
| 14 | D1 | DIO | 8-bit bidirectional data bus |
| 15 | D0 | DIO | 8-bit bidirectional data bus LSB |
| 16 | VDD2 | | + 2.8 V Supply voltage, digital |
| 17 | TOUT | DOUT | Test Output, Digital |
| 18 | XCLR | DIN | HW reset input, active state LOW |
| 19 | TMODE | DIN/pd | Test mode selection, pull-down > 50 k Ω |
| 20 | TSEL | DIN/pd | Test select, pull-down > 50 k Ω |
| 21 | XINT | DOUT | Interrupt request, active state LOW |
| 22 | SYNBIAS | DOUT | Synthesizer on/off control, HIGH = power on |
| 23 | RXBIAS | DOUT | Receiver on/off control, HIGH = power on |
| 24 | IF | AIN | IF input |
| 25 | VSS2 | | 0 V Supply voltage, digital ground |
| 26 | VSA2 | | 0 V Supply voltage, analog |
| 27 | DAF | AIN | Signal input |
| 28 | FILO | AOUT | Rxfilter output |
| 29 | EXPI | AIN | Expander input |
| 30 | EAMPBO | AOUT | Expander Amplifier B output |
| 31 | EWCI | AIN | Expander Window Comparator input |
| 32 | EXPO | AOUT | Expander output |
| 33 | VDA2 | | + 2.8 V Supply voltage, analog |
| 34 | VOLI | AIN | Volume control ampl. input (Volume) |
| 35 | XEAR | AOUT | Buffered output for handset or an accessory |
| 36 | EVGND | AIN | Earphone driver virtual ground |

Table 14. Pin list of the NASTA ASIC (continued)

| Pin no | Symbol | Pin type | Notes |
|--------|-------------|----------|---|
| 37 | EARM | AOUT | Earphone driver output |
| 38 | EARP | AOUT | Earphone driver output |
| 39 | CWCI | AIN | Compander window control input |
| 40 | DACO | AOUT | DA converter output |
| 41 | SIDEAR | AOUT | Sidetone output |
| 42 | REF | AIN | Internal analog signal ground 1.40 V |
| 43 | MIC | AIN | Microphone amplifier input |
| 44 | BIMIC | AOUT | Microphone bias current output |
| 45 | CMIC | AIN | Microphone current stabilization capacitor |
| 46 | XMIC | AIN | Audio input for a handset or an accessory |
| 47 | ATTO | AOUT | Transmit HF attenuator output (TXATT) |
| 48 | VDA1 | | + 2.8 V Supply voltage, analog |
| 49 | COMI | AIN | Compressor input |
| 50 | COMO | AOUT | Compressor output |
| 51 | EMPI | AIN | Pre emphasis input |
| 52 | EMPO | AOUT | Pre emphasis output |
| 53 | LPIN | AIN | Transmit lowpass filter input |
| 54 | ATST | AOUT | Audio Filter Test output |
| 55 | MOD | AOUT | Transmit path output |
| 56 | VSA1 | | 0 V Supply voltage, analog |
| 57 | VSS1 | | 0 V Supply voltage, digital ground |
| 58 | BUZZ | AOUT | Buzzer output |
| 59 | ATOUT | AOUT | Test pin |
| 60 | CLKOUT | COUT | 14.85 MHz system clock output |
| 61 | CLKIN | CIN | 14.85 MHz system clock input |
| 62 | CLKLCD | DOUT | Clock signal for LCD, 80 kHz, tristate when MCS1=MCS2=0 |
| 63 | CLKMCU | DOUT | Clock signal for MCU, 4.8 MHz or 2.4 MHz |
| 64 | XWR | DIN/pu | Write control signal, active state LOW, pull-up > 50 k Ω |

Transmit (TX) audio signal path

The TX audio signal is processed in the NASTA circuit and fed via the MOD line to the TX synthesizer on SYNTHESIZER module.

The NASTA ASIC contains the following stages for TX signal processing:

MICAM:

The signal input level from the microphone is 2.4mVrms nom., max. 40mVrms. The signal fed to this stage and amplified up to 200 mVrms.

TXMUX + TXAAF:

TX source selection (exmic/mic/dmmf/muted). Txaafil prevents aliasing in TXBP filter.

TXATT:

TXATT is a hands free attenuator. Maximum attenuation is selectable from four levels: -30, -27, -24 or -21 dB.

MICTRI:

MICTRI is for different microphone (phone microphone, headset and handset etc.) sensitivity compensation. It is used also for dtmf level setting. Gain 16 levels, step 0.6 dB, range -4.2 - +4.8dB.

BANDPASS:

Tx bandpass filter (300 - 3000Hz) filters high freq noise and low freq hum.

COMPR:

It compresses speech dynamic area to avoid noise at tx and radio path. It is a amplitude compressor and ratio is 2:1 in dB scale. It can be bypassed for measurement or dtmf purposes.

LIM1:

Hard limiter. It cuts the signal transients at +-439 mVpp levels.

PRE-EMP:

Pre-emphasis filter gives +6 dB/oct emphasis at the frequency band of 300 - 3000Hz.

LIM2:

Hard limiter. it cuts the signal transients at +-439mV levels.

TXLP:

The corner frequency of tx lowpass filter is 3000 Hz. Amplitude attenuation is 12 dB/oct after the corner point. Filter includes notch at 6 kHz.

TXTRI:

TXTRI is for nominal deviation tuning. Gain 8 levels, step 0.5 dB, range -+1.75dB.

TXPOSTFIL:

Postfil eliminates filter clock.

SUM:

SUM block makes d/a conversion of all generated signals. Then it sums all used signals and speech together.

WTRFIL:

This block is a lowpass filter for SAT, ST and data. Transmitter Compensation Amplifier is these too. Gain 16 levels, step 0.5 dB.

WPOSFIL:

WPOSFIL filters out the replicates of the output spectrum around WTRFIL clock frequency and its harmonics.

RECEIVE (RX) AUDIO SIGNAL PATH

The NASTA contains the following stages for RX signal processing:

RXTRI:

RXTRI is for demodulation sensitivity compensation. Gain 16 levels, step 0.5 dB, range $-+3.75$ dB.

RXAAF:

RX aa filter filters out noise and other high frequency components from the incoming signal. It prevents aliasing in SATFIL and RXFIL.

RXMUX+AAFIL:

Rxmux selects speech from DAF-pin or DTMF from generator or all mute. Aafil prevents aliasing in RXFIL.

DEEMP+ RXFIL:

Rx filter filters out high frequency noise and low frequency hum. It has de-emphasis -6 dB/oct for the received speech signal (300-3000). There is a notch at 6kHz.

EXP:

Expands the speech dynamic back to normal. It is a amplitude expander and ratio is 1:2 in dB scale. It can be bypassed for measurement or DTMF purposes.

VOL:

VOL is for earphone or accessory speaker/earphone volume control. Volume Control Amplifier. Gain 16 levels over -20 to $+17.5$ dB in 2.5 dB steps.

RXATT:

RXATT is a hands free attenuator. Maximum attenuation is selectable from four levels: -30 , -27 , -24 or -21 dB. Hands free controller (HF CONTR) measures peak-to-peak

level of the received audio and controls gains of the transmit and receive attenuators as a function of measured signal level.

EAR:

The earpiece amplifier is a single input, differential output amplifier for a ceramic earpiece.

ACC:

Buffer for accessory line is capable of driving high capacitive load. Gain and response of the buffer are fixed.

SIDEAR:

Audio output to be summed with EAR amplifier. Earphone amplifier gives extra +6dB gain to SIDEAR.

Transmitting data path

The data to be transmitted is loaded into the transmitting register DTR. From the DTR register the 8 bit data is fed into PISO-register, which changes the 8-bit data bytes to serial form. The serial NRZ-data is fed to the Manchester encoder (MANEN) and then to the summing block (SUM). Timing signals needed for data transmission are generated internally.

Receiving data path

The data from anti alias filter is connected through the comparator (DATAC) to a Manchester decoder (MANDEC) which decodes Manchester data to the NRZ (Non Return to Zero) format. The modem is synchronized to the receiving data with a digital phase locked loop (DPLL) and a word synchronization detection block (RECBUF). Data validity (DATVAL) is continuously detected (DFLAG), and this information is used internally when word synchronization detection is accepted. The serial data from the Manchester decoder is 3/5 majority voted (VOTE), BCH-decoded (BCH), corrected (CORR) and shifted to the receiver register (RREG). The final data word consists of 28 bits. 4 status bits are added to RREG to make up a 32 bit register, which is read in 8 bit bytes via status multiplexer (SMUX). The Receiver timing block (RECTIM) extracts the data from the received frames on control and voice channels and generates the data transfer interrupts (WFLAG). It also generates the repeat interrupts RFLAG. It maintains bit and word synchronization during different frames and passes the synchronization status (SFLAG) forward to the status register. On FOCC (Forward Control Channel) signalling mode it separates the multiplexed data streams (channel A and B) and Busy/Idle-information (XBOI). On FVC (Forward Voice Channel) signalling mode it extracts data repeats from voice channel message frames.

IF

The Intermediate Frequency Counter (IFCTR) is located on the modem to measure the frequency of IF signal.

AFC

The AFC makes the synthesizer fine tuning. It can be used for channel side-step also.

The AFC DA-converter output DC level tunes the RF oscillator (VCXO).

ST signalling tone generator

The signalling tone generator is two bit D/A converter that produces an 8 kHz sine wave. The tolerance of the frequency is ± 1 Hz.

Receiving SAT path

The SAT signal is filtered and amplified with a bandpass filter (SATFIL). SATFIL (Supervisory Audio Tone input FILTER) is a 6 kHz bandpass filter. It separates the 5970, 6000, 6030 Hz SAT signal from the incoming voice and noise during voice channel operation. The signal is converted to digital square wave signal with a comparator (SATCOMP). The SAT detection is executed with a digital PLL/detection circuitry (SATDET). The logic compares the SCC code given by control register bits SCC0 and SCC1 to the incoming SAT frequency and indicates the result with a status register bit (SATVAL). The regenerated SAT is then fed to summing block (SUM).

Clock divider

The main function of the the NASTA baseband clock generator is to generate a 4.8 MHz clock signal with selectable frequency shift (approx. 80 ppm) from 14.85 MHz master clock.

NHX-7 employs a 2.4 MHz clock for MCU (CLKMCU) and a 80kHz kHz clock for LCD display CLKLCD.

Standby Modes for Power Saving

The normal standby mode (receiver and synthesizer are continuously ON, audio paths OFF) is automatically activated when the circuit is initialized working in control channel (COXV = 1) and the extended standby is disabled (ESTDBY = 0).

The extended standby mode (receiver and synthesizer ON/OFF times controlled by the NASTA) is activated when the circuit is initialized working in control channel, extended standby is enabled and synthesizer and receiver hardware controls are enabled (COXV=ESTDBY=SPHE=RPHE=1). In extended standby mode the interrupts from control filler messages can be masked (FIME=1). The maximum number of consecutive received filler messages without interrupt is 31. After the interrupt the number of masked interrupts (filler) is available in SRB (RFMC0...4).

RF Section

Technical Summary

The purpose of the RF sub-module is to receive and demodulate the radio frequency signal from a base station and transmit modulated RF signal to a base station. The RF section comprises the RX-submodule, the TX submodule and the Synthesizer submodule.

EMC leakage is prevented with sheet metal boxes covering the critical blocks of the transceiver.

Basic Specification

Table 15. Basic Specifications

| Parameter | Value |
|-----------------------------------|--|
| RX frequency band | 917 – 950 MHz |
| TX frequency band | 872 – 905 MHz |
| RX LO frequency band | 962 – 995 MHz |
| Duplex spacing | 45 MHz |
| Channel numbers | 1329...2047, 0...600 |
| Number of channels | 1320 |
| Channel spacing | 25 kHz |
| TX output power | 6 levels; 6.5 (+2/-4) dBm to 26.5 (+2/-4) dBm |
| Method of frequency synthesis | Dual PLL with two UHF signals for RX LO and TX |
| Frequency control | AFC with +/- 2.5 kHz limits |
| Receiver type | Superheterodyne with double IF |
| Modulator type | FM-modulator |
| Current consumption, reception | 50 mA |
| Current consumption, standby | 30 mA |
| Current consumption, transmission | 550 mA |

RF Module Characteristics

Maximum ratings

The maximum battery voltage during transmission must not exceed 5.85 V. Higher battery voltages may destroy the power amplifier module.

Table 16. Maximum ratings

| Parameter | Value |
|------------------------------------|------------------------------------|
| Battery voltage (Ni–Mh Battery) | nom. 3.6 V, min. 3.1 V, max. 4.6 V |
| Battery voltage (Li–Ion Battery) | nom. 3.6 V, min. 3.1 V, max. 4.1 V |
| Regulated supply voltage | 2.82 V +/- 0.09V |
| Operating temperature range | -10 ... +55 deg.C |

DC Characteristics

Regulator

The PSA regulator module in the BB unit regulates voltages VA, VRX and VTX to the fixed 2.82 V level for the RF unit.

Battery Save at Reception Mode

The receiver and receiver synthesizer blocks are switched on/off during stand-by mode. This switching is controlled by the NASTA – audio module. If the received signal is strong enough, it switches PSA's VRX_ENA off for about half of time. This powers down all the receiver blocks and RX–VCO. Also the synthesizer module is switched to power off mode during battery save.

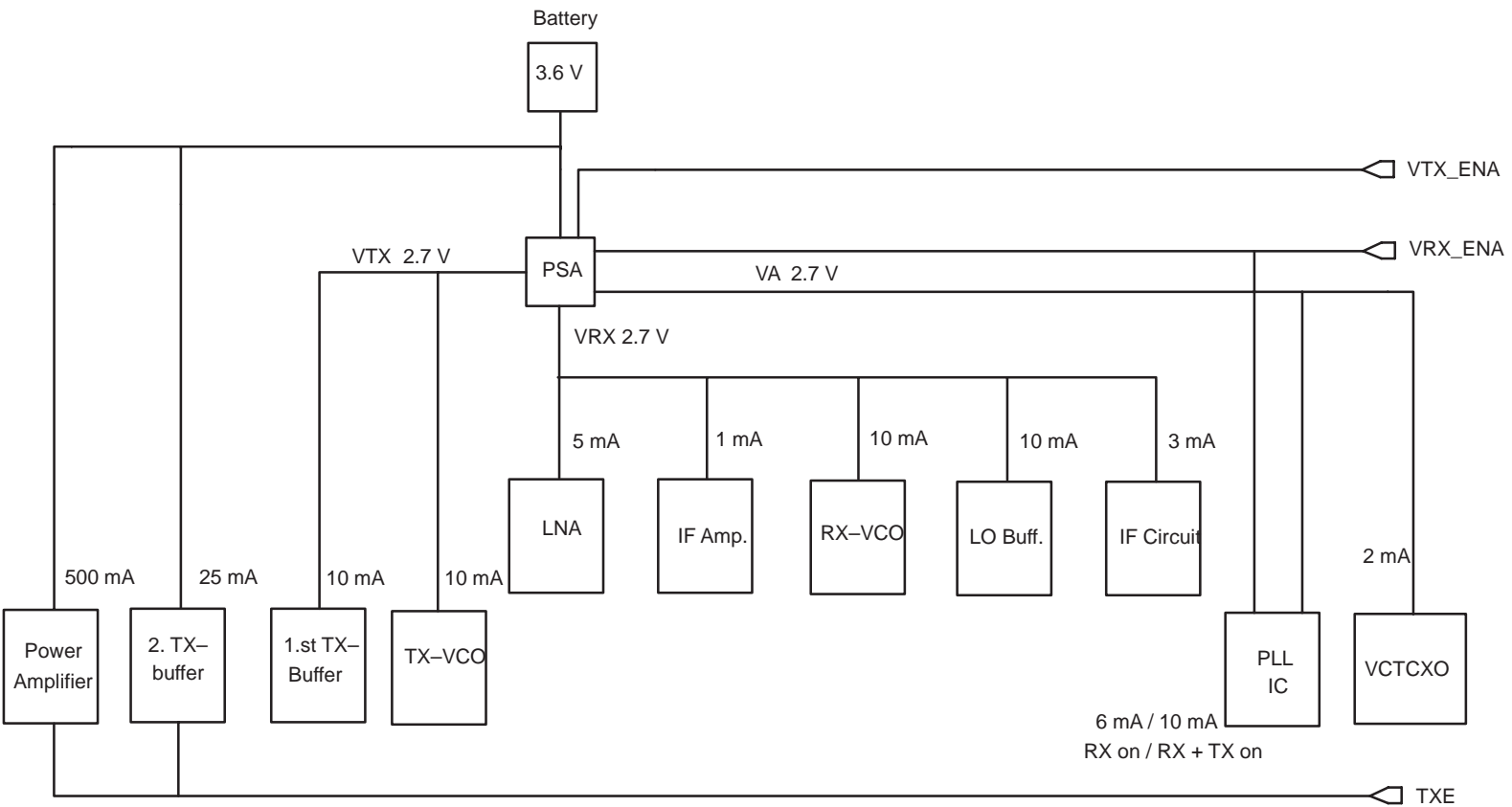
Control Signals

The following table describes the RF current consumption with different status of the control signals. RX and TX synthesizer phase locked loops are switched on/off by a control byte that is loaded to the PLL circuit.

Table 17. Control Signals and Current Consumption

| VRX_ENA + SW powerup for RX synthesizer | VTX_ENA + SW powerup for TX synthesizer | TXE | Typical Current Consumption /mA | Note |
|---|---|-----|---------------------------------|--|
| H | H | H | 550 mA | Power Level 2 |
| H | H | L | 70 mA | |
| H | L | L | 50 mA | Synthesizer TX part has been powered off |
| L | L | L | 8 mA | All RF parts have been powered off |

Power Distribution Diagram



Connections

Connections to Baseband module

| Signal Name | Type | Function |
|-------------|-------------|---|
| AFC | Analog out | The reference oscillator frequency adjust. |
| DAF | Analog in | Demodulated received signal (audio + data) |
| GND | Power | Common ground |
| IF | Analog out | 2nd IF signal (450 kHz) |
| MOD | Analog out | Modulation signal for transmitter (audio + data) |
| RSSI | Analog in | Received signal strength indicator. Voltage measurement. |
| SCLK | Digital out | Serial clock for synthesizer. Active state: Rising edge |
| SDAT | Digital out | Serial data for synthesizer. Active state: High |
| SLE | Digital out | Synthesizer latch enable. Active state: Low |
| HPD_EN | Digital out | PLL Hardware power down |
| RXS_LD | Digital in | RX–synthesizer lock detect |
| TXC | PWM out | Transmitter power control |
| TXE | Digital out | Transmitter enable. Active state: High |
| TXI | Analog in | ”TX power on” –indicator |
| VA | Power | Regulated voltage to synthesizer circuit and VCTCXO |
| VBAT | Power | Battery voltage to transmitter |
| VRX | Power | Regulated voltage to receiver |
| VTX | Power | Regulated voltage to TX–VCO, 1st.TX–LO buffer and power control circuit |

| Values for digital control signal | | |
|-----------------------------------|-----|--|
| Supply voltage | VDD | 2.7 V |
| Logical 1 | VOH | $>VDD \cdot 0,7$ |
| Logical 0 | VOL | $<VDD \cdot 0,3$ |
| Logical 1 | IOH | $<1\text{mA}$, $1\mu\text{A}$ (typical) |
| Logical 0 | IOL | $<1\text{mA}$, $1\mu\text{A}$ (typical) |

| CLKIN | VCTCXO signal | |
|----------------|---------------|---|
| Frequency | | 14.85 MHz |
| Level | | 1 Vpp (0.7 Vpp Min.) |
| Load impedance | | $\% 5\text{ k}\Omega // 20\text{ pF}$ (Typical) |
| Start time | | 45 ms after VA rising |

| AFC | VCTCXO control voltage | |
|--------------------------------|------------------------|-----------------------------|
| Type | | analog signal (DC-level) |
| Level | | 0.3...2.5 V DC |
| Source impedance | | $Z_s < 1.5 \text{ kohm}$ |
| Load impedance | | 10 kohm // 10 pF \pm 10 % |
| Control step size for TX freq. | | 100 Hz (typical) |

| DAF | Demodulated audio and data signal | |
|------------------------|-----------------------------------|-----------------------------|
| Type | | analog signal |
| Nominal level | | 50 mVrms @2,3 kHz deviation |
| Unit to unit variation | | 35 mV...65 mV |
| Source impedance | | $Z_s < 5 \text{ kohm}$ |
| Load impedance | | $Z_L > 50 \text{ kohm}$ |

| IF | 450 kHz 2nd IF signal | |
|------------------|-----------------------|--|
| Level | | 250 mVpp (typical) not specified by manufacturer |
| Source impedance | | $< 500 \ \Omega$ |
| Load impedance | | $> 7 \text{ k} \ \Omega$ |

| MOD | Modulation signal for transmitter (Audio + data) | |
|------------------|--|------------------------------|
| Type | | Analog signal |
| Nominal level | | 200 mVrms @2.3 kHz deviation |
| Load impedance | | $Z_L > 50 \text{ k}\Omega$ |
| Source impedance | | $Z_s < 2.5 \text{ k}\Omega$ |

| RSSI | Received signal strength indicator | |
|------------------|------------------------------------|-------------------------|
| DC-level | | 0.2...2.3 V |
| Source impedance | | 56 k Ω (typical) |

| SCLK | Serial clock for synthesizer | |
|-------------|------------------------------|------------------|
| Type | | digital signal |
| Pulse width | | $> 1 \text{ us}$ |

| SDAT | Serial data for synthesizer | |
|-------------|-----------------------------|------------------|
| Type | | digital signal |
| Pulse width | | $> 1 \text{ us}$ |
| VALUES: | | |

| SDAT | Serial data for synthesizer | |
|---|------------------------------------|---|
| Control byte | | x110 011x x001 11xx (x = don't care bit) |
| Reference divider | | 1188 |
| Divider formulas for RX oscillator (ch 1329...2047) | | $N = 2 * (ch - 1329) + 73361$ |
| Divider formulas for RX oscillator (ch 0...600) | | $N = 2 * ch + 78399$ |
| Divider formulas for TX oscillator (ch 1329...2047) | | $N = 2 * (ch - 1329) + 69761$ |
| Divider formulas for TX oscillator (ch 0...600) | | $N = 2 * ch + 71199$ |

| SLE | Synthesizer enable | |
|------------|---------------------------|---|
| Type | | Digital signal |
| Function | | 0 = synthesizer enabled 1 = synthesizer disabled |

| HPD_EN | PLL Hardware power down | |
|---------------|--------------------------------|---|
| Type | | Digital signal |
| Function | | 0 = Power down enabled 1 = Power down disabled |

| RXS_LD | RX-Synthesizer lock detect | |
|---------------|-----------------------------------|----------------------------|
| Type | | Digital signal |
| Function | | 0 = Unlocked 1 = Locked |

| TXC | Transmitter power control | |
|----------------------------|----------------------------------|---|
| Type | | PWM signal |
| Function | | Duty cycle of the TXC signal defines the TX power level |
| PWM frequency | | 9.4 kHz |
| Number of duty cycle steps | | 256 |
| Load impedance | | > 100 kohm |

| TXE | Transmitter on/off control | |
|------------|-----------------------------------|-------------------------|
| Type | | Digital signal |
| Function | | 0 = TX off 1 = TX on |

| TXI | "TX power on" –indicator | |
|------------------|---------------------------------|---------------------------------|
| Type | | Analog signal |
| Source impedance | | 33 k Ω |
| Level | | < 1 V = TX off > 1 V = TX on |

| VA | Regulated voltage for synthesizer | |
|---------------|--|----------------|
| Nominal value | | 2.7 V \pm 4% |
| Max. current | | 100 mA |

| VBAT | Battery voltage | |
|------------------|------------------------|--------|
| Nominal value | | 3.6 V |
| Minimum value | | 3.1 V |
| Absolute maximum | | 4.6 V |
| Max. current | | 800 mA |

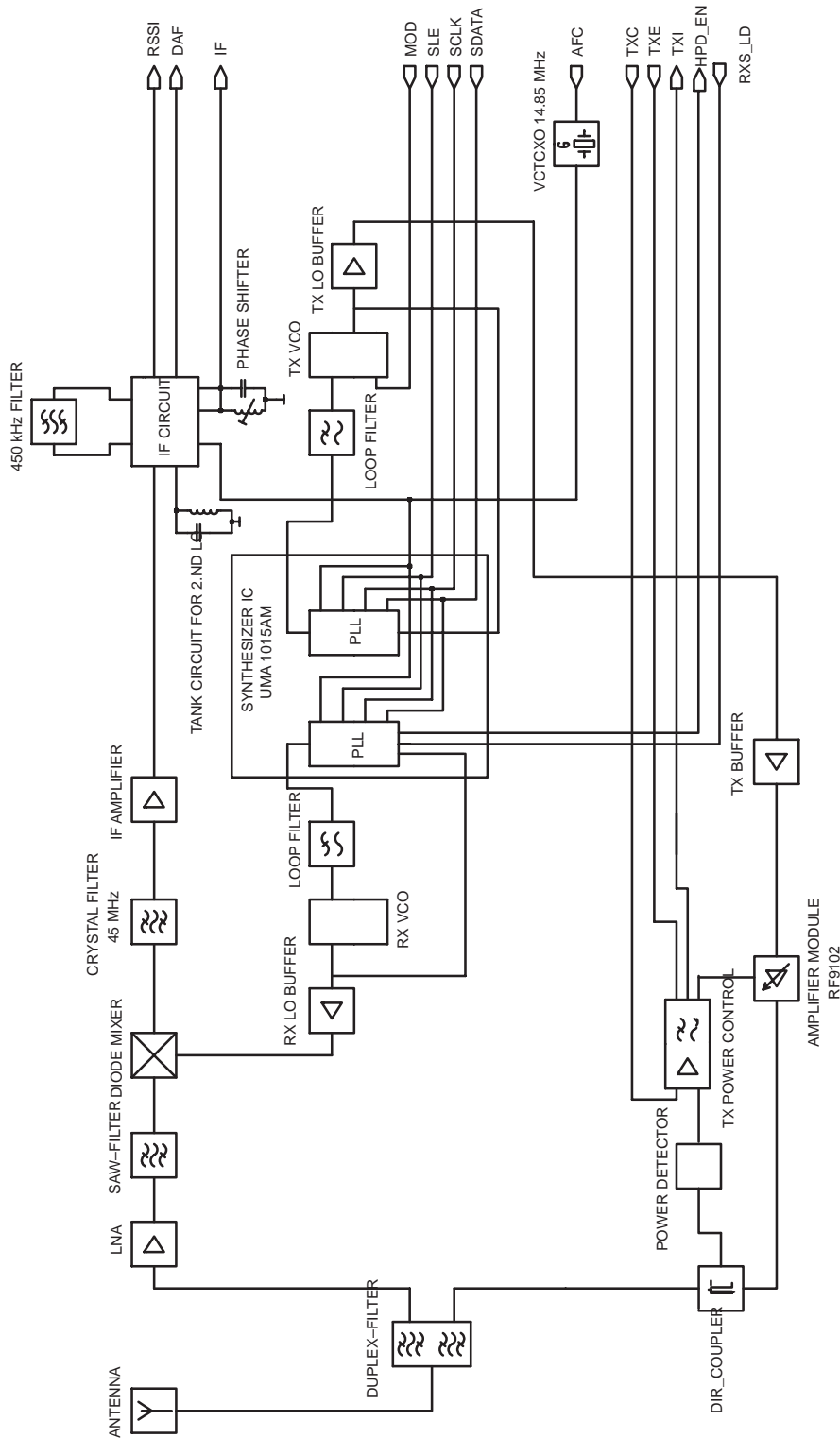
| VRX | Regulated voltage for receiver | |
|---------------|---------------------------------------|-------------------------|
| Nominal value | | 2.82 V (–0.09V /+0.08V) |
| Max. current | | 50 mA |
| VTX | Regulated voltage for TX | |
| Nominal value | | 2.82 V (–0.09V /+0.08V) |
| Max. current | | 60 mA |

Antenna

The phone includes a helix antenna. The electrical length of the helix antenna is 3/8 wave length.

Functional description of radio sub-module

Block diagram



RF components

| | |
|--------------------|----------------|
| Antenna: | 0660184 |
| Antenna clip: | 9510480 |
| Duplexer: | 4512085 |
| 45 MHz IF filter: | 4510129 |
| 450 kHz IF filter: | 4550045 |
| SAW filter: | 4511034 |
| VCTCXO: | 4510171 |
| FM detector IC: | 4349694 |
| PLL IC: | 4340393 |
| RX VCO: | 4350113 |
| TX VCO: | 4350115 |
| Power amplifier: | 4370099 |

Receiver

The receiver is a dual-conversion superheterodyne using two intermediate frequencies, 45 MHz and 450 kHz.

The RF signal from the duplexer RX port is applied to the RF amplifier.

Next the signal is filtered with SAW-filter Z321. The filter is followed by a single balanced diode mixer, which has 6 dB conversion loss.

After that mixer signal is filtered with the crystal filter Z350, which has 15 kHz bandwidth. Next the IF signal is amplified by V380. From the amplifier the IF-signal is applied to the second mixer.

The second mixer, the LO buffer transistor, IF amplifier and quadrature detector are all integrated in the circuit N370. The second LO frequency, 44.55 MHz, is third harmonic of the VCTCXO frequency. LO signal is realized with tank circuit C372 and L371. After the mixer the 450kHz IF signal is filtered with ceramic filter Z370. The IF amplifier output signal is phase shifted by resonance circuit. After this the signal is fed to a quadrature detector.

Signal DAF is low pass filtered by R372 and C379. The DAF, RSSI and 2nd IF signal (450 kHz) are fed to the audio/logic unit.

During battery-save mode the voltage VRX is down and all the receiver blocks and the RX synthesizer are powered down.

RX Synthesizer

The first injection frequency for receiver is generated by a digital phase locked loop (PLL). The output frequency of the loop (LO) is obtained from a voltage-controlled oscillator (VCO) G530. The VCO output signal is amplified by RX-LO-buffer and fed to the receiver mixer. The injection level required by the receiver mixer is about +3 dBm. In addition, the signal is fed back to the dualsynthesizer circuit N820.

The overall divisor of the chain is selected according to the desired channel.

The internal dividers of N820 are programmed with 17 bits, which are transferred serially on the SDAT (synthesizer data) line from the processor into an internal shift register also located in N820. Data transfer is timed with SCLK clock pulses.

The divided frequency is compared with a highly stable reference frequency by a phase comparator in the PLL circuit. The phase comparator controls the VCO frequency by means of a DC voltage through the loop filter so as to keep the divided frequency applied to the phase comparator equal to the fixed reference frequency.

The reference frequency is 12,5 kHz. This reference frequency is obtained from voltage controlled crystal oscillator (VCTCXO). Oscillator frequency is 14.85 MHz. The VCTCXO frequency is divided by 1188.

RX loop filter

Phase comparator output is pin 3. If the VCO (G530) frequency is too high, the output goes low and discharge integrator capacitor C521. After this, the DC control voltage and the VCO frequency will decrease.

If the VCO frequency is too low, the output goes high and charge the integrator capacitors C522 and C523. Thereafter the DC control voltage and the VCO frequency will go up.

Output pulses from the phase detector have to be supplied to the loop filter. The function of the integrator is to convert positive and negative pulses to DC voltage. The remaining ripple and AC components are filtered in the lowpass filter.

TX Synthesizer

The transmitter synthesizer generates a frequency modulated transmitter signal for the transmitter section. The modulated TX injection frequency is generated in TX-VCO (G430). The TX modulated TX signal is amplified in TX-buffer before the transmitter.

TX Loop Filter

Output pulses from the phase detector N820 pin 17 have to be supplied to the loop filter. The integrator, which consists of R420 and C421, converts positive and negative pulses to DC voltage. The remaining ripple is filtered in the low-pass filter.

Transmitter

The transmitter comprises a power amplifier module. The modulated RF signal from the TX synthesizer is applied to the 50 ohm input of the module. The power level is controlled by the voltage supplied to the pin 8. Amplifier module has two output pins (pins 13 and 12). The real part of the output impedance is 7 ohms. The amplified RF signal is fed to the duplex filter via

a 50 ohm impedance matching circuit. Harmonics generated by the transmitter are attenuated in the matching circuit and duplex filter. A voltage proportional to the output power is rectified from a directional coupler by DC-biased Schottky diode V640. This rectified voltage is fed to a differential amplifier which consists of transistor V650. The reference voltage is filtered from the PWM signal provided by the TXC line. The differential amplifier adjusts the control voltage so that the reference voltage and the voltage proportional to the output power are equal. The transmitter is switched on when TXE goes high (logic 1). TXE enables the transmitter power control circuit by transistor V641. When the transmitter is inactive (TXE low) the RF level from the transmitter is reduced below -60 dBm.

RF Characteristics

| Temperature range | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|-----------------------|---------|-------------------|---------|--------------|
| Operating temperature | -10 | | +55 | °C |

Duplexer

| | Transmitter | | Receiver | |
|-------------------------|-----------------|-----------|-----------------|-----------|
| Frequency | 872...905 MHz | | 917...950 MHz | |
| Insertion loss max | 3.5 dB | | 4.8 dB | |
| Ripple at BW max | 3.0 dB | | 3.0 dB | |
| Termination impedance | 50 Ω | | 50 Ω | |
| Permissible input power | 2.0 W | | 1.0W | |
| Returnloss at BW | 12 dB | | 10 dB | |
| | Frequency [MHz] | Att. [dB] | Frequency [MHz] | Att. [dB] |
| Attenuation min | | | | |
| | 917...950 | 40 | 872...905 | 48 |
| | 1744...1810 | 40 | 962...995 | 10 |
| | 2616...2715 | 30 | 1007...1040 | 25 |

RX submodule

RX Specification

| N=Normal E=Extreme conditions | | Unit / Notes |
|-------------------------------------|--------------------------|--------------------|
| | Frequency range | 917...950 MHz |
| | Type | FM receiver, 2 IFs |
| | Intermediate Frequencies | 45 MHz, 450 kHz |

RX Specification (continued)

| N=Normal E=Extreme conditions | | Unit / Notes |
|-------------------------------------|--|---------------------------|
| N | RF-sensitivity | < -110 dBm (SINAD 20 dB) |
| E | RF-sensitivity | < -107 dBm (SINAD 20 dB) |
| N / E | Adjacent channel selectivity | >55 dB (25 kHz) |
| N | Spurious response rejection | > 55 dB |
| N | Intermodulation rejection | > 55 dB |
| | Blocking: | |
| N | RX-band excluding the receive freq ± 1 MHz | >-50 dBm |
| N | Bands 895 – 905 MHz and 970 – 980 MHz | > -23 dBm |
| N | Spurious emissions: | |
| N | 100 kHz ... 1000 MHz | < -57 dBm |
| N | 1000 MHz ... 4000 MHz | < -47 dBm |
| N | RX-band | < -70 dBm |
| N | TX-band | < -60 dBm |
| N / E | Audio harmonic distortion | < -30 dB (third harmonic) |
| N/E | Noise & Hum | < -32 dB |
| | Audio frequency response | |
| N | 300 Hz...500 Hz | +0.5/-1 dBm |
| N | 500 Hz...2 kHz | ± 0.5 dB |
| N | 2 kHz... 3 kHz | +0.5/-1 dB |
| N | 10 kHz | -6 dB (max.) |
| N / E | RSSI dynamic range | > 65 dB |
| N / E | RSSI starting level | > -113 dBm / -110 dBm |
| N/E | RSSI linearity | < 5 (10) dB |

Preamplifier

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|---------------------|---------|-------------------|---------|--------------|
| Supply voltage | | 2.7 | | V |
| Frequency band | 917 | | 950 | MHz |
| Current consumption | | 5.5 | 6.5 | mA |
| Insertion gain | 14 | 15 | 16 | dB |
| Gain flatness | | $\pm 0,5$ | | dB |
| Noise figure | | | 2.3 | dB |
| Reverse isolation | 20 | | | dB |

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|--|---------|-------------------|---------|--------------|
| IIP3 | -8,0 | | | dBm |
| Input return loss ($Z_0=50\Omega$) | 10 | | | dB |
| Output return loss ($Z_0=50\Omega$) | 10 | | | dB |

SAW-filter

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|-------------------------|---------|-------------------|---------|--------------|
| Center frequency, f_0 | | 933,5 | | MHz |
| Bandwidth | | $\pm 16,5$ | | MHz |
| Attenuation: | | | | |
| DC – 850MHz | 35 | | | dB |
| 850 – 900 MHz | 25 | | | dB |
| 900 – 905 MHz | 10 | | | dB |
| 962 – 970 MHz | 8 | | | dB |
| 970 – 1007 MHz | 18 | | | dB |
| 1007 – 1010 MHz | 30 | | | dB |
| 1010 MHz – 1.5 GHz | 35 | | | dB |
| 1.5 – 3.0 GHz | 15 | | | dB |
| Insertion loss | | 4.0 | 5.0 | dB |
| Passband ripple | | | 1.0 | dB |
| VSWR in passband | | | 2.5 | |
| Termination impedance | | 50 | | Ω |

1st mixer

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|-----------------|---------|-------------------|---------|--------------|
| Frequency band | | | | |
| RF | 917 | | 950 | MHz |
| LO | 962 | | 995 | MHz |
| IF | | 45 | | MHz |
| Conversion loss | | | 9 | dB |
| IIP3 | 5 | | | dBm |
| LO power level | 3 | 5 | 7 | dBm |
| LO–RF isolation | 22 | 30 | | dB |

1st IF-filter

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|-----------------------------|------------------|-------------------|---------|-----------------------------|
| Type | | | | 2-pole |
| Center frequency, f_0 | | 45,000 | | MHz |
| Passband width (at -3dB) | $f_0 \pm 15$ kHz | | | kHz |
| Stopband attenuation | 12 | | | dB at $f_0 \pm 50$ kHz |
| Stopband attenuation | 65 | | | dB at $f_0 - 900$ kHz |
| Spurious response rejection | 10 | | | dB |
| Insertion loss | | | 3 | dB |
| Passband ripple | | | 1 | dB |
| Terminating impedance | | 800 // 1,5 | | Ω // pF |
| Group delay distortion | | 10 | | μ s at $f_0 \pm 15$ kHz |
| Case | | | | SMD |

IF-amplifier

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|--------------------------|---------|-------------------|---------|----------------|
| Operating frequency | | 45 | | MHz |
| Supply voltage | 2,7 | | 3,0 | V |
| Input impedance | | 800 // 1.5 | | Ω // pF |
| Output impedance | | 1000 | | Ω |
| Current consumption | | 1 | | mA |
| Insertion gain (voltage) | | 10 | | dB |
| Noise figure | | | 3 | dB |
| IIP3 | -30 | | | dBm |

2nd IF filter

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|------------------|------------|-------------------|----------|--------------|
| Center frequency | | 450 | | kHz |
| 6 dB bandwidth | ± 12.5 | | | kHz |
| 50 dB bandwidth | | | ± 24 | kHz |
| Insertion loss | | | 4.0 | dB |

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|-----------------------------|---------|-------------------|---------|--------------|
| Ripple | | | 3.0 | dB |
| Spurious response rejection | 35 | | | dBm |
| Input & output impedance | | 1500 | | Ω |

IF-circuit

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|---------------------------|---------|-------------------|---------|------------------------------|
| Supply voltage | 2.0 | | 2.6 | V |
| Current consumption | | | 4.6 | mA |
| Input resistance | | 5500 | | Ω |
| Input capacitance | | 2,8 | | pF |
| Mixer output resistance | -20 % | 1800 | +20 % | Ω |
| Noise figure | | | 10 | dB at 45 MHz |
| 3rd order intercept point | -11 | | | dBm |
| Mixer conversion gain | 15 | 18 | 21 | dB |
| 2. lo frequency | | 44.550 | | MHz |
| 2. lo injection level | 90 | | | dB μ V |
| 2. lo input impedance | 10 | | | k Ω |
| 2. lo harmonic level | | | -6 | dBc |
| AM-rejection | | 40 | | dB ($V_{in}=80$ dB μ V) |
| RSSI dynamic range | 60 | | | dB |
| Case | | | | 16 SSOP |

TX submodule

TX Specification

| N=Normal E=Extreme conditions | | Unit / Notes |
|-------------------------------------|--|---------------------|
| | Frequency range | 872 ... 905 MHz |
| N / E | Output power (after duplex filter) at all channels | |
| N / E | PL 0,1,2 | 26.5 (+2/ -4) dBm |
| N / E | PL 3 | 22.5 (+2/ -4) dBm |
| N / E | PL 4 | 18.5 (+2/ -4) dBm |
| N / E | PL 5 | 14.5 (+2/ -4) dBm |

TX Specification (continued)

| N=Normal E=Extreme conditions | | Unit / Notes |
|-------------------------------------|---|---------------------|
| N / E | PL 6 | 10.5 (+2/ -4) dBm |
| N / E | PL 7 | 6.5 (+2/ -4) dBm |
| N / E | Carrier switching time to within ± 3 dB of specified output power and frequency within ± 2.5 ppm of final frequency | < 2 ms |
| N / E | Carrier switching time from full power to -60 dBm | < 2 ms |
| N / E | Power level transition time (within 3 dB from any power level) | < 20 ms |
| | Spurious emissions | |
| N | 100 kHz ... 1000 MHz | < -36 dBm |
| N | 1000 MHz ... 4000 MHz | < -30 dBm |
| N | RX-band | < -70 dBm |
| N | TX-band (except ± 50 kHz Ft) | < -36 dBm |
| | Modulation bandwidth outside the region | |
| N | ± 17 kHz | < -26 dBc |
| N | ± 37.5 kHz | < -45 dBc |
| N | ± 50 kHz | < -60 dBc |

Power amplifier

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|--------------------------------|---------|-------------------|-----------|---|
| Supply voltage | 3.15 | 3.6 | 5.85 | V |
| Current consumption | | 550 | | mA (at $P_{out} = 1,2$ W) |
| Input power | +4 | +6 | +9 | dBm |
| Output power | 30 | 31 | 33 | dBm |
| Efficiency | 50 | | | % (at operation point) |
| Harmonic level | | | -30 | dBc (at $2 \cdot f_{carrier}$) |
| Harmonic level | | | -45 | dBc (at $3 \cdot f_{carrier}$ and higher) |
| Spurious mixing loss at output | 9 | 10 | | dB ($f_{carrier} \pm 45$ MHz) |
| Output SWR | | | No damage | |

Power control circuit

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|---------------------|---------|-------------------|---------|--------------|
| Supply voltage | 3.15 | 3.6 | 4.6 | V |
| Drive current | | | 10 | mA |
| Power control range | 20 | | | dB |

Synthesizer submodule

PLL circuit for RX local oscillator signal and TX injection

PLL Synthesizer specification

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|---------------------------------------|---------|-------------------|-----------|---------------------------------|
| Frequency band (RX LO) | 962 | | 995 | MHz |
| Frequency band (TX) | 872 | | 905 | MHz |
| Channel separation | | 25 | | kHz |
| VCTCXO frequency | | 14.85 | | MHz |
| VCTCXO input level | | 1 | | V _{pp} (10k Ω) |
| Frequency stability | | | ± 2.5 | ppm |
| RF signal level from VCO to prescaler | 50 | | | mV _{rms} |
| Supply voltage | 2.7 | | | V |
| Current consumption | | 8.5 | | mA |

RX local oscillator signal

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|------------------------------------|---------|-------------------|---------|----------------------|
| Frequency band | 962 | | 995 | MHz |
| Output level | +3 | +5 | +7 | dBm / 50 Ω |
| Output return loss | | 10 | | dB |
| Phase noise | | -112 | | dBc / Hz (25 kHz) |
| Tuning voltage limits | 1 | | 4 | V |
| Tuning voltage at center frequency | | 2.5 | | V |
| Tuning voltage sensitivity | 15 | 18 | 21 | MHz / V |
| Temperature stability | | ± 10 | | MHz (all conditions) |
| Locking time to ± 1 channel | | | 20 | ms |

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|---------------------------------------|---------|-------------------|---------|-------------------|
| Locking time to any channel | | | 40 | ms |
| RF signal level from VCO to prescaler | 50 | | | mV _{rms} |
| Supply voltage | 2.7 | | | V |
| Current consumption | | 22 | | mA |

TX VCO

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|---------------------------------------|---------|-------------------|---------|----------------------------------|
| Frequency band | 872 | | 905 | MHz |
| Output level | -3 | 0 | +3 | dBm / 50 Ω |
| Output return loss | | 10 | | dB |
| Phase noise | | -102 | | dBc / Hz (25 kHz) |
| Tuning voltage limits | 0 | | 4 | V |
| Tuning voltage at center frequency | | 2,5 | | V |
| Tuning voltage sensitivity | 15 | 18 | 21 | MHz / V |
| Locking time to ± 1 channel | | | 20 | ms |
| Locking time to any channel | | | 40 | ms |
| Modulation | | | | |
| Input impedance | | 100 | | kΩ |
| deviation error | | | ±10 | % (in all conditions) |
| mod. frequency | 0,3 | | 10 | kHz |
| mod. sensitivity | | 200 | | mV _{rms} (2.3 kHz dev.) |
| RF signal level from VCO to prescaler | 50 | | | mV _{rms} |
| Supply voltage | 2.7 | | | V |
| Current consumption | | 10 | | mA |

TX buffers

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|-----------------|---------|-------------------|---------|--------------|
| Frequency range | 872 | | 905 | MHz |
| 1.st buffer | | | | |
| Output level | -2 | | 4 | dBm |

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|---------------------|---------|-------------------|---------|--------------|
| Supply voltage | 2.7 | | | V |
| Current consumption | | 10 | | mA |
| 2.nd buffer | | | | |
| Output level | 8 | | 12 | dBm |
| Supply voltage | 3.1 | 3.6 | 4.6 | V |
| Current consumption | | 35 | | mA |

VCTCXO

| | Minimum | Typical / Nominal | Maximum | Unit / Notes |
|---------------------------|---------|-------------------|-----------|----------------------|
| Frequency | | 14.85 | | MHz |
| Control voltage | 0.5 | | 2,5 | V |
| Controlled frequency area | | $f_0 \pm 1,25$ | | Hz |
| Control step | | 1.5 | | Hz |
| Frequency accuracy | | | ± 2.5 | ppm (all conditions) |
| Output level | | 1 | | Vpp |
| Supply voltage | 2.7 | | | V |
| Current consumption | | 2 | | mA |

Parts list of JP3 (EDMS Issue 4.3)

Code: 0201185

| ITEM | CODE | DESCRIPTION | VALUE | TYPE |
|------|---------|---------------|-------|------------------|
| R102 | 1422881 | Chip resistor | 0.22 | 5 % 1 W 1218 |
| R105 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R106 | 1430187 | Chip resistor | 47 k | 1 % 0.063 W 0402 |
| R107 | 1430764 | Chip resistor | 3.3 k | 5 % 0.063 W 0402 |
| R110 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R111 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R140 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R141 | 1430788 | Chip resistor | 22 k | 5 % 0.063 W 0402 |
| R142 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R143 | 1430145 | Chip resistor | 100 k | 1 % 0.063 W 0402 |
| R144 | 1430145 | Chip resistor | 100 k | 1 % 0.063 W 0402 |
| R145 | 1430842 | Chip resistor | 680 k | 1 % 0.063 W 0402 |
| R146 | 1430842 | Chip resistor | 680 k | 1 % 0.063 W 0402 |
| R147 | 1430788 | Chip resistor | 22 k | 5 % 0.063 W 0402 |
| R148 | 1430766 | Chip resistor | 3.9 k | 5 % 0.063 W 0402 |
| R149 | 1430780 | Chip resistor | 12 k | 5 % 0.063 W 0402 |
| R161 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R162 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R163 | 1430734 | Chip resistor | 220 | 5 % 0.063 W 0402 |
| R172 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R202 | 1430145 | Chip resistor | 100 k | 1 % 0.063 W 0402 |
| R203 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R206 | 1430754 | Chip resistor | 1.0 k | 5 % 0.063 W 0402 |
| R207 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R208 | 1430690 | Chip jumper | | 0402 |
| R210 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R211 | 1430776 | Chip resistor | 8.2 k | 5 % 0.063 W 0402 |
| R212 | 1430690 | Chip jumper | | 0402 |
| R231 | 1430121 | Chip resistor | 22 k | 1 % 0.063 W 0402 |
| R232 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R241 | 1430790 | Chip resistor | 27 k | 5 % 0.063 W 0402 |
| R251 | 1430792 | Chip resistor | 33 k | 5 % 0.063 W 0402 |
| R252 | 1430792 | Chip resistor | 33 k | 5 % 0.063 W 0402 |
| R261 | 1430754 | Chip resistor | 1.0 k | 5 % 0.063 W 0402 |
| R262 | 1430832 | Chip resistor | 2.7 k | 5 % 0.063 W 0402 |
| R320 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R322 | 1430744 | Chip resistor | 470 | 5 % 0.063 W 0402 |
| R323 | 1430772 | Chip resistor | 5.6 k | 5 % 0.063 W 0402 |
| R333 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R340 | 1430776 | Chip resistor | 8.2 k | 5 % 0.063 W 0402 |
| R341 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R342 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R343 | 1430734 | Chip resistor | 220 | 5 % 0.063 W 0402 |

| | | | | |
|------|---------|---------------|-------|------------------|
| R361 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R362 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R363 | 1430756 | Chip resistor | 1.2 k | 5 % 0.063 W 0402 |
| R366 | 1430714 | Chip resistor | 33 | 5 % 0.063 W 0402 |
| R370 | 1430758 | Chip resistor | 1.5 k | 5 % 0.063 W 0402 |
| R371 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R372 | 1430762 | Chip resistor | 2.2 k | 5 % 0.063 W 0402 |
| R373 | 1430714 | Chip resistor | 33 | 5 % 0.063 W 0402 |
| R381 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R420 | 1430774 | Chip resistor | 6.8 k | 5 % 0.063 W 0402 |
| R421 | 1430786 | Chip resistor | 18 k | 5 % 0.063 W 0402 |
| R422 | 1430690 | Chip jumper | | 0402 |
| R423 | 1430690 | Chip jumper | | 0402 |
| R430 | 1430718 | Chip resistor | 47 | 5 % 0.063 W 0402 |
| R431 | 1430734 | Chip resistor | 220 | 5 % 0.063 W 0402 |
| R434 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R440 | 1430720 | Chip resistor | 56 | 5 % 0.063 W 0402 |
| R441 | 1430774 | Chip resistor | 6.8 k | 5 % 0.063 W 0402 |
| R442 | 1430764 | Chip resistor | 3.3 k | 5 % 0.063 W 0402 |
| R443 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R444 | 1430744 | Chip resistor | 470 | 5 % 0.063 W 0402 |
| R450 | 1430726 | Chip resistor | 100 | 5 % 0.063 W 0402 |
| R451 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R452 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R453 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R454 | 1430724 | Chip resistor | 82 | 5 % 0.063 W 0402 |
| R455 | 1430690 | Chip jumper | | 0402 |
| R520 | 1430774 | Chip resistor | 6.8 k | 5 % 0.063 W 0402 |
| R521 | 1430784 | Chip resistor | 15 k | 5 % 0.063 W 0402 |
| R522 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R523 | 1430690 | Chip jumper | | 0402 |
| R530 | 1430724 | Chip resistor | 82 | 5 % 0.063 W 0402 |
| R531 | 1430734 | Chip resistor | 220 | 5 % 0.063 W 0402 |
| R532 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R641 | 1430726 | Chip resistor | 100 | 5 % 0.063 W 0402 |
| R642 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R643 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R644 | 1430690 | Chip jumper | | 0402 |
| R645 | 1430792 | Chip resistor | 33 k | 5 % 0.063 W 0402 |
| R646 | 1430770 | Chip resistor | 4.7 k | 5 % 0.063 W 0402 |
| R647 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R648 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R651 | 1430796 | Chip resistor | 47 k | 5 % 0.063 W 0402 |
| R652 | 1430786 | Chip resistor | 18 k | 5 % 0.063 W 0402 |
| R653 | 1430754 | Chip resistor | 1.0 k | 5 % 0.063 W 0402 |
| R654 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R655 | 1430808 | Chip resistor | 150 k | 5 % 0.063 W 0402 |

| | | | | |
|------|---------|------------------------------|-------|------------------|
| R656 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R658 | 1430690 | Chip jumper | | 0402 |
| R659 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R660 | 1430690 | Chip jumper | | 0402 |
| R731 | 1430766 | Chip resistor | 3.9 k | 5 % 0.063 W 0402 |
| R741 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R742 | 1430762 | Chip resistor | 2.2 k | 5 % 0.063 W 0402 |
| R743 | 1430796 | Chip resistor | 47 k | 5 % 0.063 W 0402 |
| R745 | 1430762 | Chip resistor | 2.2 k | 5 % 0.063 W 0402 |
| R746 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R747 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R752 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R753 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R754 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R755 | 1430710 | Chip resistor | 22 | 5 % 0.063 W 0402 |
| R760 | 1430812 | Chip resistor | 220 k | 5 % 0.063 W 0402 |
| R767 | 1430764 | Chip resistor | 3.3 k | 5 % 0.063 W 0402 |
| R768 | 1430794 | Chip resistor | 39 k | 5 % 0.063 W 0402 |
| R769 | 1430796 | Chip resistor | 47 k | 5 % 0.063 W 0402 |
| R770 | 1430788 | Chip resistor | 22 k | 5 % 0.063 W 0402 |
| R771 | 1430776 | Chip resistor | 8.2 k | 5 % 0.063 W 0402 |
| R775 | 1430690 | Chip jumper | | 0402 |
| R777 | 1430690 | Chip jumper | | 0402 |
| R790 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R791 | 1430788 | Chip resistor | 22 k | 5 % 0.063 W 0402 |
| R792 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R793 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R794 | 1430804 | Chip resistor | 100 k | 5 % 0.063 W 0402 |
| R795 | 1430726 | Chip resistor | 100 | 5 % 0.063 W 0402 |
| R796 | 1430796 | Chip resistor | 47 k | 5 % 0.063 W 0402 |
| R797 | 1430812 | Chip resistor | 220 k | 5 % 0.063 W 0402 |
| R811 | 1430754 | Chip resistor | 1.0 k | 5 % 0.063 W 0402 |
| R812 | 1430754 | Chip resistor | 1.0 k | 5 % 0.063 W 0402 |
| R816 | 1430700 | Chip resistor | 10 | 5 % 0.063 W 0402 |
| R820 | 1430792 | Chip resistor | 33 k | 5 % 0.063 W 0402 |
| R821 | 1430690 | Chip jumper | | 0402 |
| R822 | 1430690 | Chip jumper | | 0402 |
| R826 | 1430788 | Chip resistor | 22 k | 5 % 0.063 W 0402 |
| R829 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R830 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| R831 | 1430778 | Chip resistor | 10 k | 5 % 0.063 W 0402 |
| C100 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C101 | 2604127 | Tantalum cap. 3.5x2.8x1.9 | 1.0 u | 20 % 35 V |
| C102 | 2604209 | Tantalum cap. 3.2x1.6x1.6 | 1.0 u | 20 % 16 V |
| C103 | 2611668 | Tantalum cap. | 4.7 u | 20 % 10 V |

Baseband Module JP3

Technical Documentation

| | | | |
|-------------|---------|---------------|------------------------|
| 3.2x1.6x1.6 | | | |
| C104 | 2604209 | Tantalum cap. | 1.0 u 20 % 16 V |
| 3.2x1.6x1.6 | | | |
| C105 | 2604209 | Tantalum cap. | 1.0 u 20 % 16 V |
| 3.2x1.6x1.6 | | | |
| C106 | 2604209 | Tantalum cap. | 1.0 u 20 % 16 V |
| 3.2x1.6x1.6 | | | |
| C107 | 2604209 | Tantalum cap. | 1.0 u 20 % 16 V |
| 3.2x1.6x1.6 | | | |
| C108 | 2604209 | Tantalum cap. | 1.0 u 20 % 16 V |
| 3.2x1.6x1.6 | | | |
| C111 | 2320530 | Ceramic cap. | 5.6 p 0.25 % 50 V 0402 |
| C112 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C113 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C114 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C115 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C116 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C117 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C118 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C119 | 2320546 | Ceramic cap. | 27 p 5 % 50 V 0402 |
| C120 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C121 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C122 | 2320584 | Ceramic cap. | 1.0 n 5 % 50 V 0402 |
| C123 | 2320620 | Ceramic cap. | 10 n 5 % 16 V 0402 |
| C124 | 2320131 | Ceramic cap. | 33 n 10 % 16 V 0603 |
| C125 | 2604209 | Tantalum cap. | 1.0 u 20 % 16 V |
| 3.2x1.6x1.6 | | | |
| C126 | 2320083 | Ceramic cap. | 1.0 n 5 % 50 V 0603 |
| C127 | 2320560 | Ceramic cap. | 100 p 5 % 50 V 0402 |
| C128 | 2320107 | Ceramic cap. | 10 n 5 % 50 V 0603 |
| C129 | 2320546 | Ceramic cap. | 27 p 5 % 50 V 0402 |
| C130 | 2320546 | Ceramic cap. | 27 p 5 % 50 V 0402 |
| C131 | 2320546 | Ceramic cap. | 27 p 5 % 50 V 0402 |
| C132 | 2320546 | Ceramic cap. | 27 p 5 % 50 V 0402 |
| C133 | 2320620 | Ceramic cap. | 10 n 5 % 16 V 0402 |
| C140 | 2320131 | Ceramic cap. | 33 n 10 % 16 V 0603 |
| C141 | 2320131 | Ceramic cap. | 33 n 10 % 16 V 0603 |
| C161 | 2320546 | Ceramic cap. | 27 p 5 % 50 V 0402 |
| C201 | 2307816 | Ceramic cap. | 47 n 20 % 25 V 0805 |
| C202 | 2307816 | Ceramic cap. | 47 n 20 % 25 V 0805 |
| C203 | 2307816 | Ceramic cap. | 47 n 20 % 25 V 0805 |
| C210 | 2320781 | Ceramic cap. | 47 n 20 % 16 V 0603 |
| C228 | 2320620 | Ceramic cap. | 10 n 5 % 16 V 0402 |
| C229 | 2320620 | Ceramic cap. | 10 n 5 % 16 V 0402 |
| C231 | 2320779 | Ceramic cap. | 100 n 10 % 16 V 0603 |
| C232 | 2320620 | Ceramic cap. | 10 n 5 % 16 V 0402 |
| C251 | 2307816 | Ceramic cap. | 47 n 20 % 25 V 0805 |

| | | | | |
|------|---------|------------------------------|-------|------------------|
| C260 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C261 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C262 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C263 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C264 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C265 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C266 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C267 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C268 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C269 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C270 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C271 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C272 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C273 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C274 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C275 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C276 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C277 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C278 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C279 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C280 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C281 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C320 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C321 | 2320532 | Ceramic cap. | 6.8 p | 0.25 % 50 V 0402 |
| C322 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C324 | 2320538 | Ceramic cap. | 12 p | 5 % 50 V 0402 |
| C325 | 2320534 | Ceramic cap. | 8.2 p | 0.25 % 50 V 0402 |
| C328 | 2611668 | Tantalum cap. 3.2x1.6x1.6 | 4.7 u | 20 % 10 V |
| C331 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C340 | 2320520 | Ceramic cap. | 2.2 p | 0.25 % 50 V 0402 |
| C341 | 2320538 | Ceramic cap. | 12 p | 5 % 50 V 0402 |
| C342 | 2320526 | Ceramic cap. | 3.9 p | 0.25 % 50 V 0402 |
| C343 | 2320526 | Ceramic cap. | 3.9 p | 0.25 % 50 V 0402 |
| C344 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C345 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C350 | 2320544 | Ceramic cap. | 22 p | 5 % 50 V 0402 |
| C354 | 2320530 | Ceramic cap. | 5.6 p | 0.25 % 50 V 0402 |
| C360 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C361 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C362 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C370 | 2320584 | Ceramic cap. | 1.0 n | 5 % 50 V 0402 |
| C371 | 2320584 | Ceramic cap. | 1.0 n | 5 % 50 V 0402 |
| C372 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C373 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C374 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C375 | 2604329 | Tantalum cap. | 4.7 u | 20 % 10 V |

3.5x2.8x1.9

| | | | | |
|------|---------|---------------|-------|----------------|
| C376 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C377 | 2310490 | Ceramic cap. | 360 p | 2 % 50 V 0805 |
| C378 | 2320556 | Ceramic cap. | 68 p | 5 % 50 V 0402 |
| C379 | 2320584 | Ceramic cap. | 1.0 n | 5 % 50 V 0402 |
| C380 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C381 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C382 | 2320560 | Ceramic cap. | 100 p | 5 % 50 V 0402 |
| C420 | 2320120 | Ceramic cap. | 22 n | 10 % 25 V 0603 |
| C421 | 2604209 | Tantalum cap. | 1.0 u | 20 % 16 V |

3.2x1.6x1.6

| | | | | |
|------|---------|---------------|-------|---------------|
| C424 | 2320618 | Ceramic cap. | 4.7 n | 5 % 25 V 0402 |
| C430 | 2611668 | Tantalum cap. | 4.7 u | 20 % 10 V |

3.2x1.6x1.6

| | | | | |
|------|---------|---------------|-------|------------------|
| C431 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C432 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C440 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C442 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C443 | 2320530 | Ceramic cap. | 5.6 p | 0.25 % 50 V 0402 |
| C444 | 2320520 | Ceramic cap. | 2.2 p | 0.25 % 50 V 0402 |
| C447 | 2320602 | Ceramic cap. | 4.7 p | 0.25 % 50 V 0402 |
| C448 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C449 | 2320602 | Ceramic cap. | 4.7 p | 0.25 % 50 V 0402 |
| C450 | 2320514 | Ceramic cap. | 1.2 p | 0.25 % 50 V 0402 |
| C451 | 2320514 | Ceramic cap. | 1.2 p | 0.25 % 50 V 0402 |
| C452 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C453 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C454 | 2320532 | Ceramic cap. | 6.8 p | 0.25 % 50 V 0402 |
| C455 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C520 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C522 | 2310784 | Ceramic cap. | 100 n | 10 % 25 V 0805 |
| C523 | 2320781 | Ceramic cap. | 47 n | 20 % 16 V 0603 |
| C524 | 2320594 | Ceramic cap. | 2.7 n | 5 % 50 V 0402 |
| C525 | 2320618 | Ceramic cap. | 4.7 n | 5 % 25 V 0402 |
| C530 | 2611668 | Tantalum cap. | 4.7 u | 20 % 10 V |

3.2x1.6x1.6

| | | | | |
|------|---------|---------------|-------|------------------|
| C531 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C532 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C601 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C602 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C603 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C604 | 2320602 | Ceramic cap. | 4.7 p | 0.25 % 50 V 0402 |
| C605 | 2604209 | Tantalum cap. | 1.0 u | 20 % 16 V |

3.2x1.6x1.6

| | | | | |
|------|---------|---------------|-------|---------------|
| C606 | 2320584 | Ceramic cap. | 1.0 n | 5 % 50 V 0402 |
| C625 | 2604209 | Tantalum cap. | 1.0 u | 20 % 16 V |

3.2x1.6x1.6

| | | | | |
|------|---------|------------------------------|-------|------------------|
| C631 | 2320532 | Ceramic cap. | 6.8 p | 0.25 % 50 V 0402 |
| C633 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C634 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C635 | 2320530 | Ceramic cap. | 5.6 p | 0.25 % 50 V 0402 |
| C641 | 2320532 | Ceramic cap. | 6.8 p | 0.25 % 50 V 0402 |
| C642 | 2320538 | Ceramic cap. | 12 p | 5 % 50 V 0402 |
| C643 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C644 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C645 | 2320548 | Ceramic cap. | 33 p | 5 % 50 V 0402 |
| C646 | 2320598 | Ceramic cap. | 3.9 n | 5 % 50 V 0402 |
| C648 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C650 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C652 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C660 | 2320602 | Ceramic cap. | 4.7 p | 0.25 % 50 V 0402 |
| C701 | 2320584 | Ceramic cap. | 1.0 n | 5 % 50 V 0402 |
| C703 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C704 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C705 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C706 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C710 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C711 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C712 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C713 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C714 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C715 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C716 | 2310784 | Ceramic cap. | 100 n | 10 % 25 V 0805 |
| C717 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C721 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C731 | 2320546 | Ceramic cap. | 27 p | 5 % 50 V 0402 |
| C732 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C733 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C740 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C741 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C742 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C753 | 2320584 | Ceramic cap. | 1.0 n | 5 % 50 V 0402 |
| C760 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C762 | 2320779 | Ceramic cap. | 100 n | 10 % 16 V 0603 |
| C763 | 2604209 | Tantalum cap. 3.2x1.6x1.6 | 1.0 u | 20 % 16 V |
| C766 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |
| C767 | 2320620 | Ceramic cap. | 10 n | 5 % 16 V 0402 |
| C770 | 2320594 | Ceramic cap. | 2.7 n | 5 % 50 V 0402 |
| C771 | 2320764 | Ceramic cap. | 6.8 n | 10 % 25 V 0402 |
| C772 | 2320109 | Ceramic cap. | 15 n | 5 % 25 V 0603 |
| C781 | 2320779 | Ceramic cap. | 100 n | 10 % 16 V 0603 |
| C790 | 2320779 | Ceramic cap. | 100 n | 10 % 16 V 0603 |
| C791 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 |

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|------|-------------|-----------------------------------|---------------|------------------|-------|
| C792 | 2312296 | Ceramic cap. | | Y5 V 1210 | |
| C793 | 2320131 | Ceramic cap. | 33 n | 10 % 16 V 0603 | |
| C794 | 2320779 | Ceramic cap. | 100 n | 10 % 16 V 0603 | |
| C812 | 2604209 | Tantalum cap. | 1.0 u | 20 % 16 V | |
| | 3.2x1.6x1.6 | | | | |
| C813 | 2320534 | Ceramic cap. | 8.2 p | 0.25 % 50 V 0402 | |
| C814 | 2320598 | Ceramic cap. | 3.9 n | 5 % 50 V 0402 | |
| C815 | 2320598 | Ceramic cap. | 3.9 n | 5 % 50 V 0402 | |
| C820 | 2320618 | Ceramic cap. | 4.7 n | 5 % 25 V 0402 | |
| C821 | 2611668 | Tantalum cap. | 4.7 u | 20 % 10 V | |
| | 3.2x1.6x1.6 | | | | |
| C823 | 2604209 | Tantalum cap. | 1.0 u | 20 % 16 V | |
| | 3.2x1.6x1.6 | | | | |
| C824 | 2320598 | Ceramic cap. | 3.9 n | 5 % 50 V 0402 | |
| C825 | 2604209 | Tantalum cap. | 1.0 u | 20 % 16 V | |
| | 3.2x1.6x1.6 | | | | |
| C826 | 2320598 | Ceramic cap. | 3.9 n | 5 % 50 V 0402 | |
| L101 | 3641262 | Ferrite bead 30r/100mhz 2a | 1206 | 1206 | |
| L102 | 3641262 | Ferrite bead 30r/100mhz 2a | 1206 | 1206 | |
| L103 | 3641262 | Ferrite bead 30r/100mhz 2a | 1206 | 1206 | |
| L104 | 3641262 | Ferrite bead 30r/100mhz 2a | 1206 | 1206 | |
| L320 | 3645111 | Chip coil | 3 n | Q=8/100M 0603 | |
| L350 | 3645015 | Chip coil | 560 n | 10 % Q=15/25 MHz | |
| | 0603 | | | | |
| L360 | 3608439 | Chip coil | 820 n | 5 % 1206 | |
| L361 | 3608439 | Chip coil | 820 n | 5 % 1206 | |
| L370 | 3640103 | Chip coil | 320 u | 2 % Q=40/796 kHz | |
| | 1812 | | | | |
| L371 | 3641302 | Chip coil | 470 n | 5 % Q=30/25 MHz | |
| | 1008 | | | | |
| L430 | 3641262 | Ferrite bead 30r/100mhz 2a | 1206 | 1206 | |
| L631 | 3641262 | Ferrite bead 30r/100mhz 2a | 1206 | 1206 | |
| G430 | 4350115 | Vco 872–905mhz 3.0v 10ma tx etacs | | | ETACS |
| G520 | 4350113 | Vco 962–995mhz 3.0v 10ma rx etacs | | | ETACS |
| G810 | 4510171 | VCTCXO | 14.85 M | +–2PPM 3.0V | |
| F101 | 5119011 | SM, fuse f2a 63v | 120 | 1206 | |
| F102 | 5119011 | SM, fuse f2a 63v | 120 | 1206 | |
| Z100 | 3640035 | Filt z>450r/100m 0r7max 0.2a 0603 | | 0603 | |
| Z101 | 3640035 | Filt z>450r/100m 0r7max 0.2a 0603 | | 0603 | |
| Z102 | 3640035 | Filt z>450r/100m 0r7max 0.2a 0603 | | 0603 | |
| Z103 | 3640035 | Filt z>450r/100m 0r7max 0.2a 0603 | | 0603 | |
| Z104 | 3640035 | Filt z>450r/100m 0r7max 0.2a 0603 | | 0603 | |
| Z321 | 4511034 | Saw filter | 933.5+–16.5 M | 5.4x4.7 | |
| Z350 | 4510129 | XTAL filter | 45 M | +–15KHZ | SMD |
| Z370 | 4550045 | Cer.filt 450+–12.5khz/6db11.8x7.5 | | | |
| Z660 | 4512085 | Dupl 872–905/917–950mhz | 29x14 | 29x14 | |
| V101 | 1825005 | Chip varistor vwm14v vc30v | 0805 | 0805 | |

| | | | |
|------|---------|-------------------------------------|------------------------------------|
| V102 | 1825003 | Chip varistor vwm5.5v vc15.5 0805 | 0805 |
| V103 | 4113651 | Trans. supr. | QUAD 6 V SOT23-5 |
| V120 | 4100567 | Sch. diode x 2 | BAS70-04 70V15 mA SER-SOT23 |
| V140 | 4219922 | Transistor x 2 | UM6 |
| V200 | 4210102 | Transistor | BC858W npn 30 V 100 mA 200MWSOT323 |
| V210 | 4100567 | Sch. diode x 2 | BAS70-04 70V15 mA SER-SOT23 |
| V320 | 4210004 | Transistor | BFG67X npn 20 V 50 mA 7.5GHZSOT143 |
| V340 | 4115802 | Sch. diode x 2 | 4V 30 mA SOT23 |
| V341 | 4210090 | Transistor | BFG540/X npn 15 V 129 mA SOT143 |
| V380 | 4210066 | Transistor BFR93AWnnpn 12 V 35 mA | SOT323 |
| V430 | 4210066 | Transistor BFR93AWnnpn 12 V 35 mA | SOT323 |
| V440 | 4210090 | Transistor BFG540/Xnnpn 15 V 129 mA | SOT143 |
| V640 | 4110014 | Sch. diode x 2 | BAS70-07 70 V 15 mA SOT143 |
| V641 | 4219922 | Transistor x 2 | UM6 |
| V650 | 4219904 | Transistor x 2 | UMX1 npn 40 V SOT363 |
| V651 | 4210102 | Transistor BC858Wpnp 30 V 100 mA | 200MW SOT323 |
| V740 | 4210100 | Transistor BC848W npn 30 V | SOT323 |
| V741 | 4100567 | Sch. diode x 2 BAS70-04 70V15 mA | SERSOT23 |
| V790 | 4219922 | Transistor x 2 | UM6 |
| D002 | 4340251 | IC, EEPROM | NMP40251 SO8S |
| D700 | 4340387 | IC, 2xbilateral switch sso TC7W66FU | SSOP8 |
| N100 | 4370165 | Chaps charger control so16 | SO16 |
| N101 | 4370471 | Power asic for etacs/nmt450 | |
| N140 | 4340059 | IC, lp opamp+3/15v r&r ssoLMC7101 | SSOP5 |
| N370 | 4349694 | IC, if amp+fm detector sso TA31136 | SSO16 |
| N601 | 4370099 | Rf9102 pw amp 824-849mhz | SO16SQB |
| N701 | 4370469 | Nasta 4.5 mas1020a | |
| N761 | 4340331 | IC, Power amp. | LM4862 P W SO8S |
| N820 | 4340393 | IC, 2xsynth 1.1ghz ssopUMA1015AM | SSOP20 |
| X099 | 5460021 | SM, conn 2x14m spring p1.0 pcb/p | PCB/PCB |
| X101 | 5469069 | SM, batt conn 2pol spr p3.5 100v | 100V2A |
| X102 | 5469069 | SM, batt conn 2pol spr p3.5 100v | 100V2A |
| X103 | 5469061 | SM, system conn 6af+3dc+mic+jack | |
| A300 | 9517011 | Shield assembly-4 | dmc00508 |
| A400 | 9517010 | Shield assembly-3 | dmc00507 |
| A500 | 9517010 | Shield assembly-3 | dmc00507 |
| A600 | 9517011 | Shield assembly-4 | dmc00508 |
| | 9510480 | Antenna clip | dmd04121 nhx-7 |
| | 9854322 | PCB JP3 41.0X111.95X1.0 | M4 4/PA |
| | 0240775 | SW program MCU | for NHX-7 |

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